NPA1020-DE

12.5 – 14.5 GHz GaN 15 W Power Amplifier

Product Description

The Nxbeam NPA1020-DE is a Ku-band high power amplifier MMIC fabricated in 0.2um GaN HEMT on SiC. This part is ideally suited for Ku-band satellite communications applications. The MMIC operates from 12.5 to 14.5 GHz and provides 15 W saturated output power, 40% PAE, and 25 dB of linear gain.

The NPA1020-DE comes in die form with RF input and output matched to 50 Ω with DC blocking capacitors for easy system integration. The HEMT devices are fully passivated for reliable operation. Bond pad and backside metallization are Au-based for compatibility with eutectic die attachment methods.

Key Features

- Frequency: 12.5 – 14.5 GHz
- Linear Gain (Ave.): 25 dB
- Psat: 15 W
- PAE (Ave.): 40%
- Chip Dimensions: 5.0 x 2.6 x 0.1 mm

Electrical Specifications

Test Condition: Vd = 24 V, Idq = 0.2 A, Pulsed On-Wafer Data, Typical Performance at 25°C

Parameter		Min	Typical	Max	Unit
Frequency		12.5		14.5	GHz
Gain (Small Signal)	12.5 GHz		24		dB
	13.5 GHz		26.4		
	14.5 GHz		24.7		
Output Power (at Psat, Pin=18 dBm)	12.5 GHz		41.9		dBm
	13.5 GHz		42.4		
	14.5 GHz		41.9		
PAE (at Psat, Pin=18 dBm)	12.5 GHz		39.2		%
	13.5 GHz		38.5		
	14.5 GHz		40.5		
Power Gain (at Psat, Pin=18 dBm)	12.5 GHz		23.9		dB
	13.5 GHz		24.4		
	14.5 GHz		23.9		
Input Return Loss	12.5 GHz		12		dB
	13.5 GHz		14		
	14.5 GHz		12		
Output Return Loss	12.5 GHz		13		dB
	13.5 GHz		20		
	14.5 GHz		9		

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Absolute Maximum Ratings (Temp. = 25°C)

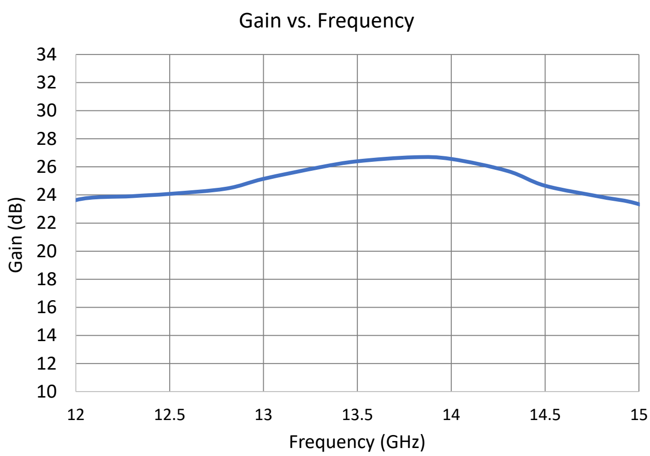
Parameter	Min	Max	Unit
Drain Voltage (Vd1, Vd2, Vd3)		28	V
Drain Current (Id1)		280	mA
Drain Current (Id2)		880	mA
Drain Current (Id3)		2160	mA
Gate Voltage (Vg1, Vg2, Vg3)	-7	0	V
Input Power (Pin)		TBD	dBm
Assembly Temperature (30 seconds)		320	°C

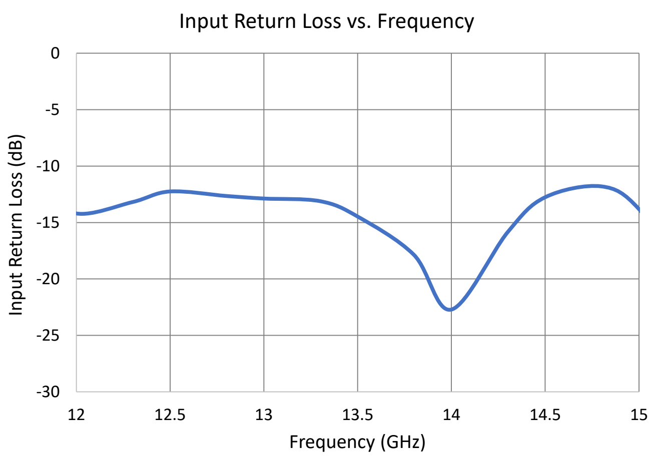
Recommended Operating Condition

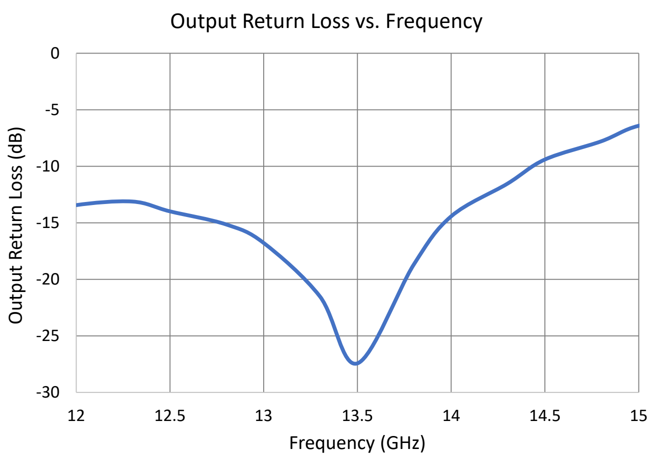
Parameter	Value	Unit
Drain Voltage (Vd)	20 - 28	V
Drain Current (Idq)	up to 1.3	A
Gate Voltage (Vg) (Typical)	-3.8	V

Small Signal Performance

Test Condition: Vd = 24 V, Idq = 0.2 A, (Pulsed On-Wafer Data, Typical Performance at 25°C)







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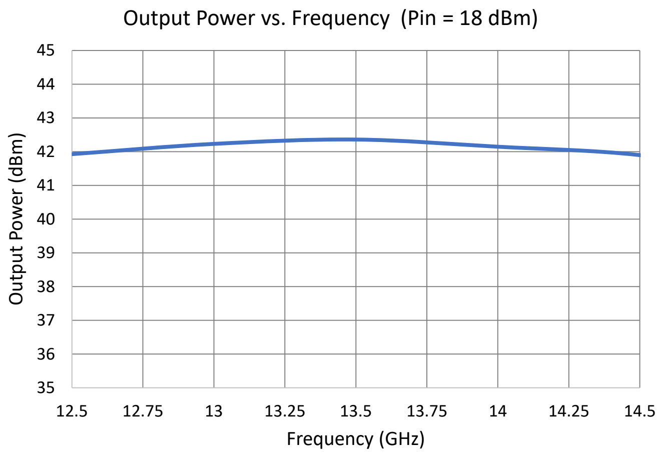
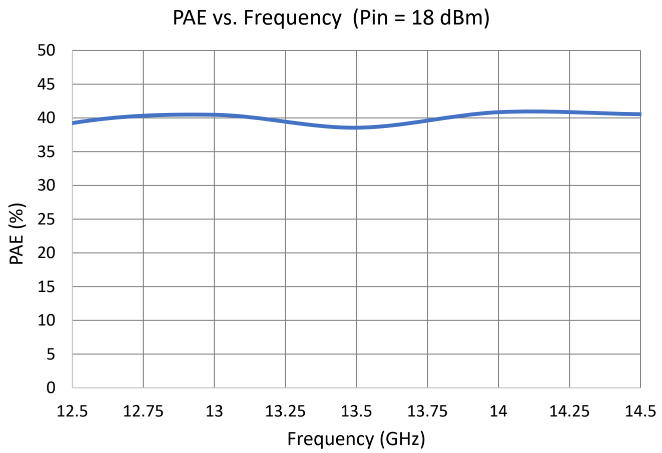
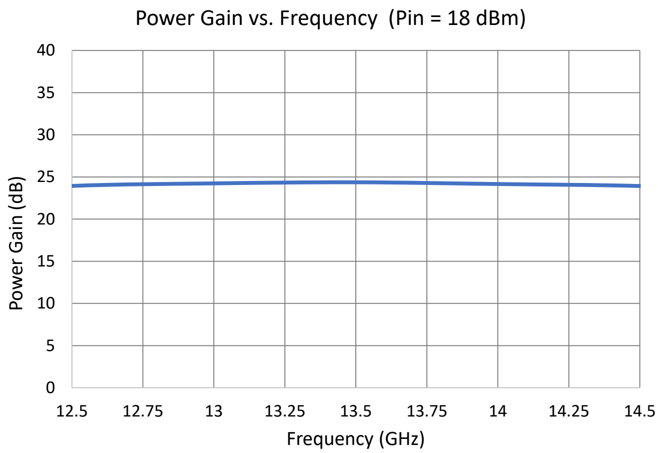
Large Signal Performance

Test Condition: Vd = 24 V, Idq = 0.2 A, Pin = 18 dBm
(Pulsed-Power On-Wafer Data, Typical Performance at 25°C)







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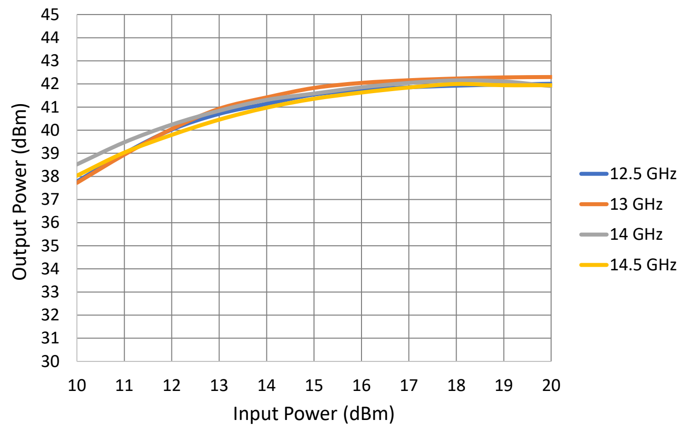
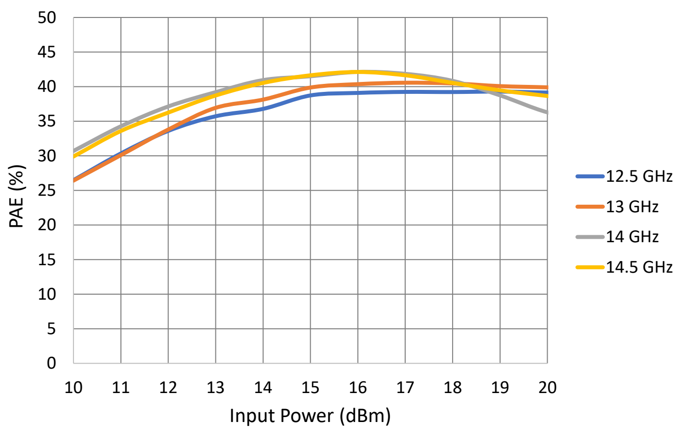
Large Signal Performance

Test Condition: Vd = 24 V, Idq = 0.2 A,
(Pulsed-Power On-Wafer Data, Typical Performance at 25°C)

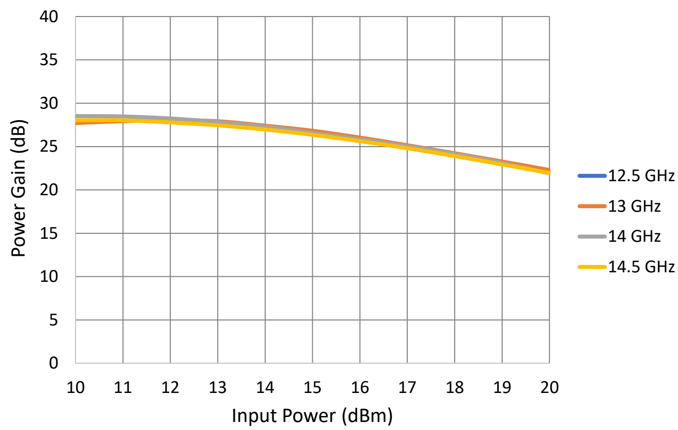
Output Power vs. Input Power vs. Frequency



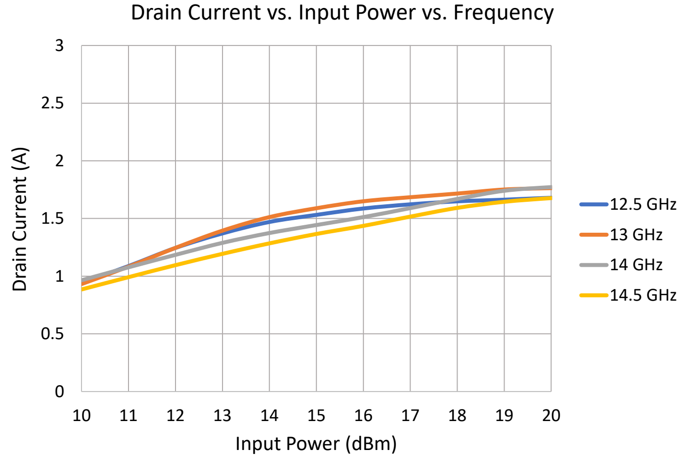
PAE vs. Input Power vs. Frequency



Power Gain vs. Input Power vs. Frequency



Drain Current vs. Input Power vs. Frequency



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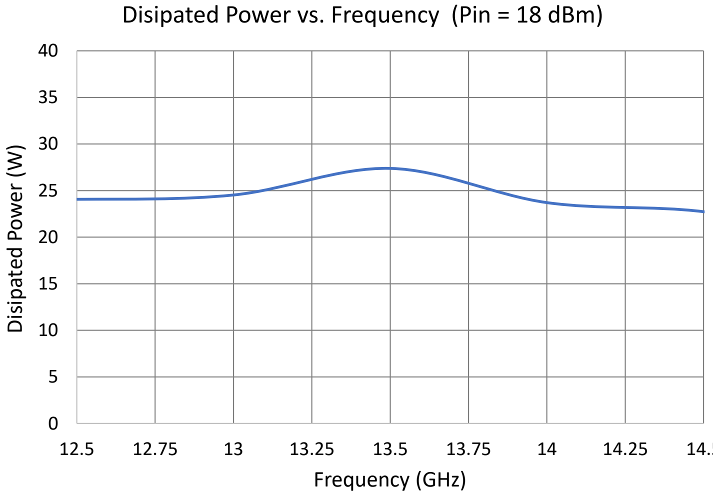
Thermal Information

RF = Off

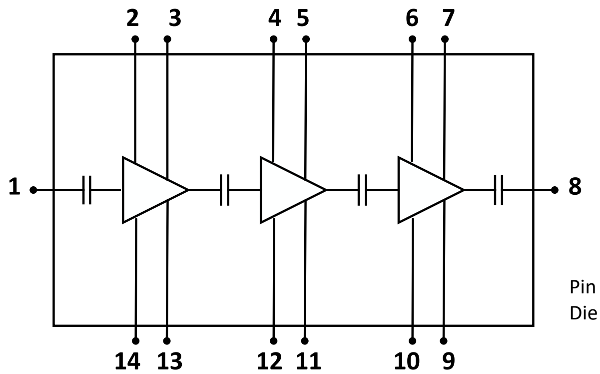
Parameter	Condition	Value	Unit
Thermal Resistance ($R_{\Theta JC}$)	RF=OFF	2.2	°C/W
Junction Temperature (Tj)	$T_{backside}$=85 °C, V_d=24 V, I_{dq}=0.2 A, P_{dis}=4.8 W	95.5	°C

RF = On, Peak Junction Temperature at Pin = 18 dBm, Psat

Parameter	Condition	Value	Unit
Thermal Resistance ($R_{\Theta JC}$)	P_{in}=18 dBm, Freq.=13.5 GHz	2.37	°C/W
Junction Temperature (Tj)	$T_{backside}$=85 °C, V_d=24 V, I_d=1.86 A, P_{dis}=27.4 W	149.8	°C



Circuit Block Diagram



Pin number information detailed under Die Size and Bond Pad Information

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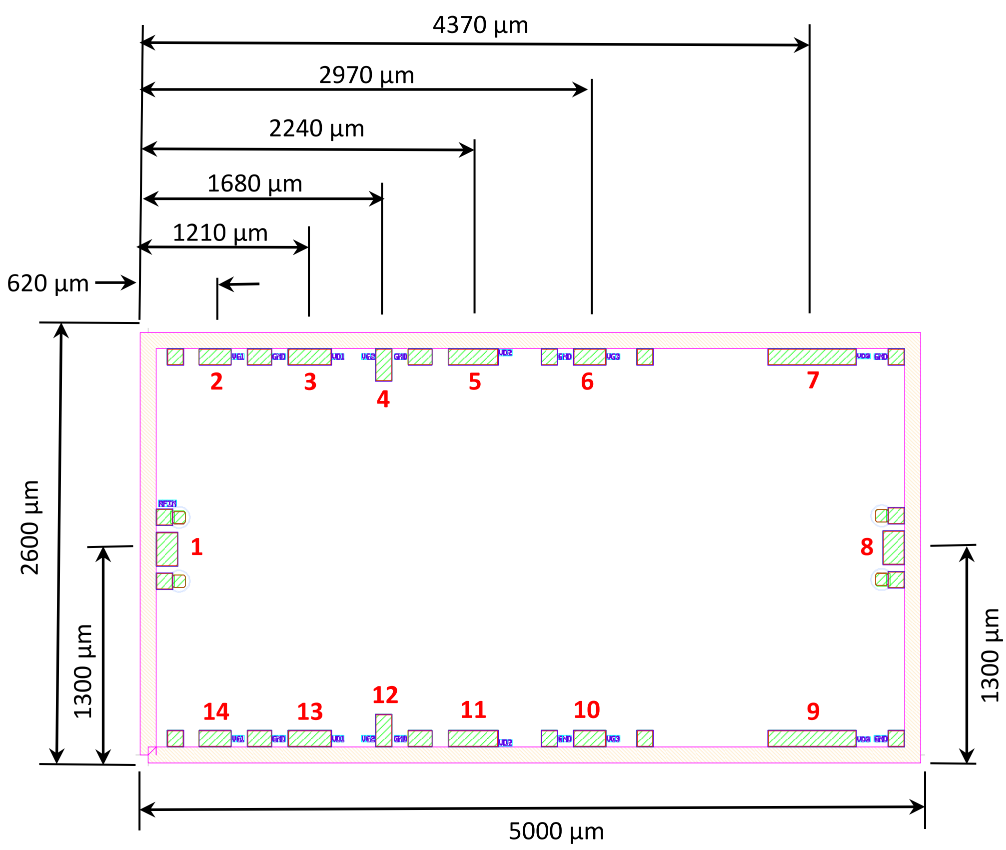
Die Size and Bond Pad Information

Chip Size = 5000 ±25 um x 2600 ±25 um
Chip Thickness = 100 um
Chip Backside metal is ground

RF Input/Output Pad Dimensions = 134 um x 208 um
DC Pad Dimensions:
- Vg1 = 200 um x 100 um
- Vg2 = 100 um x 200 um
- Vg3 = 200 um x 100 um
- Vd1 = 275 um x 100 um
- Vd2 = 310 um x 100 um
- Vd3 = 550 um x 100 um

Pad Num.	Function
1	RF in
2, 14	Vg1
3, 13	Vd1
4, 12	Vg2
5, 11	Vd2
6, 10	Vg3
7, 9	Vd3
8	RF out



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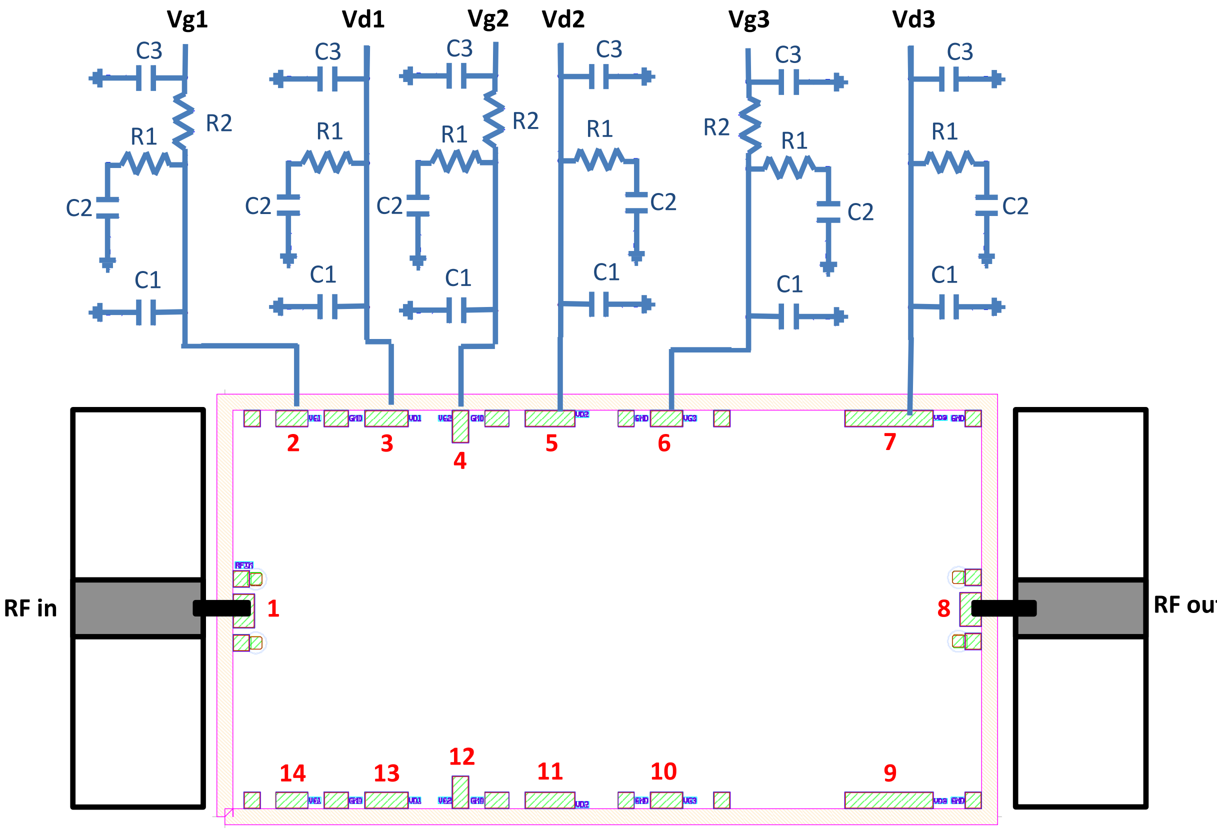
Suggested Off-Chip Components

The following diagram is a suggested bonding arraignment with off-chip components. It is also possible to tie all gate voltages together as well as all drain voltages together. This chip can be biased from either one side or both sides.



Off-Chip Component Values

Capacitor	Value
C1	100 pF
C2	0.01 µF
C3	1 µF

Resistor	Value
R1	10 Ω
R2	100 Ω

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Assembly Process

- This product has gold backside metallization and can be mounted using either a high thermal conductive epoxy or AuSn attachment.
- Nxbeam recommends the use of AuSn attachment due to the high power level of this product
- Maximum recommended temperature during die attachment is 320 °C for 14.5 seconds.
- This product contains metal air bridges so caution should be taken when handling the die to avoid damage.

Bias Information

The NPA1020-DE can be biased from either one side or both sides of the chip.

Bias-up Procedure:

1.) It is recommended that voltage and current limits are set on the voltage supply's prior to biasing the product.
2.) Ensure power supplies are properly grounded to the product test fixture.
3.) Apply negative gate voltage (-6 V) to ensure all devices are pinched off.
4.) Gradually increase the drain bias voltage to the desired bias level but not to exceed the maximum voltage of 28 V.
5.) Gradually increase the gate voltage while monitoring the drain current until the desired drain current is achieved.
6.) Apply RF signal.

Bias-down Procedure:

1.) Turn off RF signal.
2.) Gradually decrease the gate voltage down to -6 V.
3.) Gradually decrease the drain voltage down to 0 V.
4.) Gradually increase gate voltage to 0 V.
5.) Turn off supply voltages

ESD Sensitive Product

Important Information

The data contained in this document is based on pulsed on-wafer measurements. Nxbeam Inc. reserves the right to update and change without notice the characteristic data and other specifications as they apply to this document. Customers should obtain and verify the most recent product information before placing orders. Nxbeam Inc. assumes no responsibility or liability whatsoever for the use of the information contained herein.

The product represented by this datasheet is subject to U.S. Export Law as contained in ITAR or the EAR regulations.

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