

Product Description

The Nxbeam NPA2002-DE is a Ka-band high power amplifier MMIC fabricated in 0.2um GaN HEMT on SiC. The MMIC operates from 27 to 30 GHz and provides an average of 34 W saturated output power, 31% PAE, and 25 dB of linear gain. The NPA2002-DE comes in die form with RF input and output matched to 50 Ω with DC blocking capacitors for easy system integration. The HEMT devices are fully passivated for reliable operation. Bond pad and backside metallization are Au-based for compatibility with eutectic die attachment methods.



Applications

- Ka-band Satellite Communications
- 5G Infrastructure
- Point-to-Point/Multipoint Digital Radios

Key Features

- Frequency: 27 – 30 GHz
- Linear Gain (Ave.): 25 dB
- Psat (Ave.): 34 W
- PAE (Ave.): 31%
- Chip Dimensions: 5.0 x 4.0 x 0.1 mm

Electrical Specifications

Test Condition: $V_d = 24$ V, $I_{dq} = 2.0$ A, CW Performance in Fixture, Typical Performance at 25°C

Parameter		Min	Typical	Max	Unit
Frequency		27		30	GHz
Gain (Small Signal)	27 GHz		25.5		dB
	28 GHz		25.2		
	29 GHz		24.9		
	30 GHz		25.2		
Output Power (at Psat, Pin=26 dBm)	27 GHz		46.0		dBm
	28 GHz		45.4		
	29 GHz		44.9		
	30 GHz		45.0		
PAE (at Psat, Pin=26 dBm)	27 GHz		33.1		%
	28 GHz		30.8		
	29 GHz		28.6		
	30 GHz		29.6		
Power Gain (at Psat, Pin=26 dBm)	27 GHz		20.7		dB
	28 GHz		20.5		
	29 GHz		19.6		
	30 GHz		20.1		
Input Return Loss	27 GHz		15		dB
	28 GHz		12		
	29 GHz		20		
	30 GHz		18		
Output Return Loss	27 GHz		13		dB
	28 GHz		17		
	29 GHz		15		
	30 GHz		14		

Absolute Maximum Ratings (Temp. = 25°C)

Parameter	Min	Max	Unit
Drain Voltage (Vd1, Vd2, Vd3)		28	V
Drain Current (Id1)		720	mA
Drain Current (Id2)		1440	mA
Drain Current (Id3)		5720	mA
Gate Voltage (Vg1, Vg2, Vg3)	-8	0	V
Input Power (Pin)		TBD	dBm

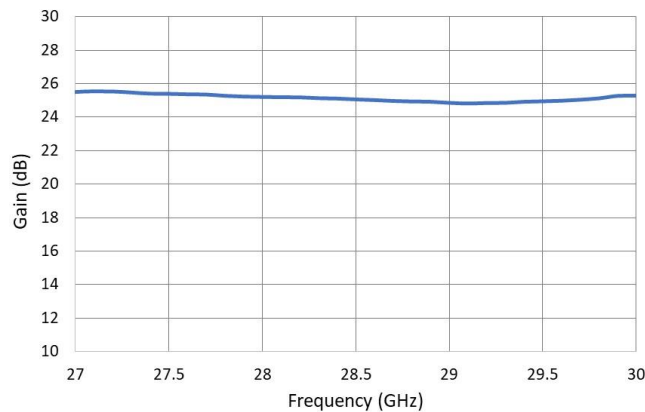
Recommended Operating Condition

Parameter	Value	Unit
Drain Voltage (Vd)	20 - 28	V
Drain Current (Idq)	up to 3.2	A
Gate Voltage (Vg) (Typical)	-4.1	V

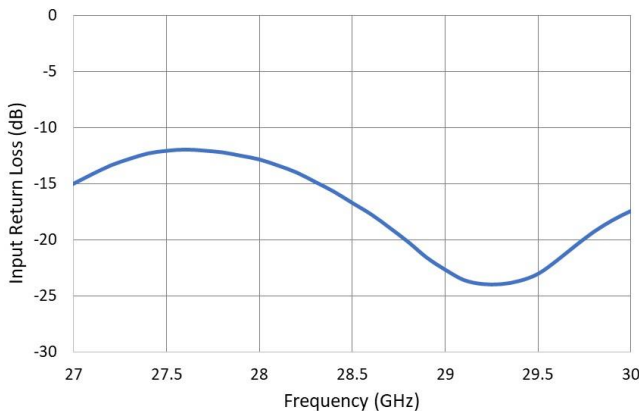
Small Signal Performance

Test Condition: Vd = 24 V, Idq = 2.0 A, (CW Performance in Fixture, Typical Performance at 25°C)

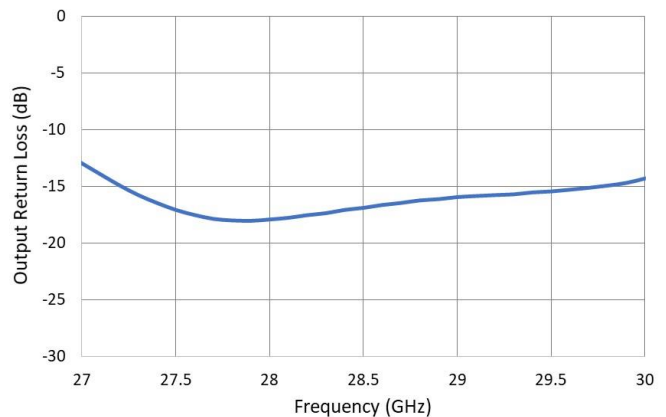
Gain vs. Frequency



Input Return Loss vs. Frequency

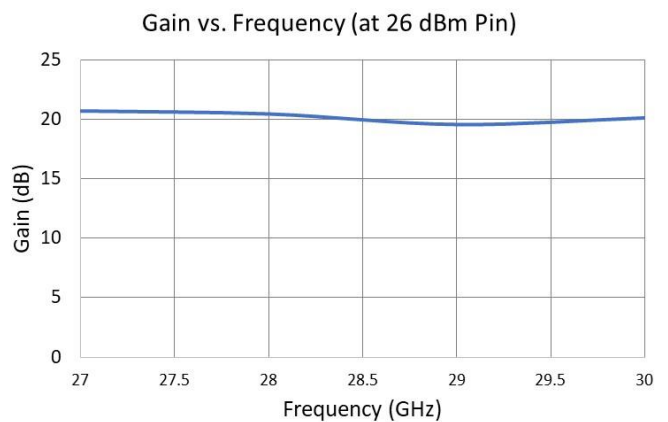
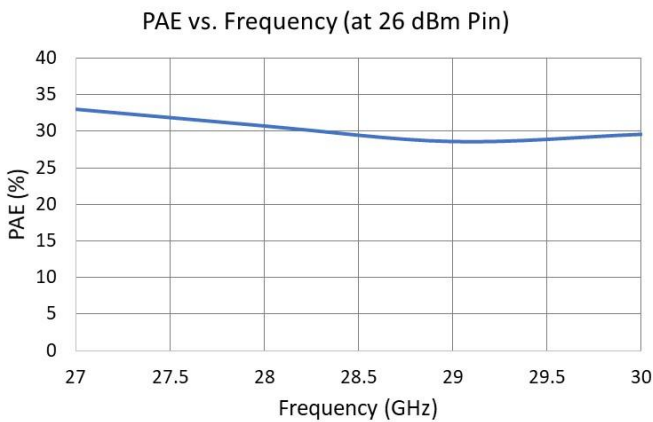
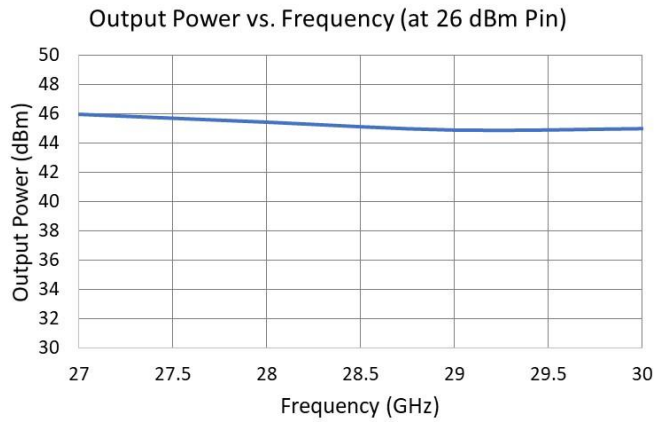


Output Return Loss vs. Frequency



Large Signal Performance

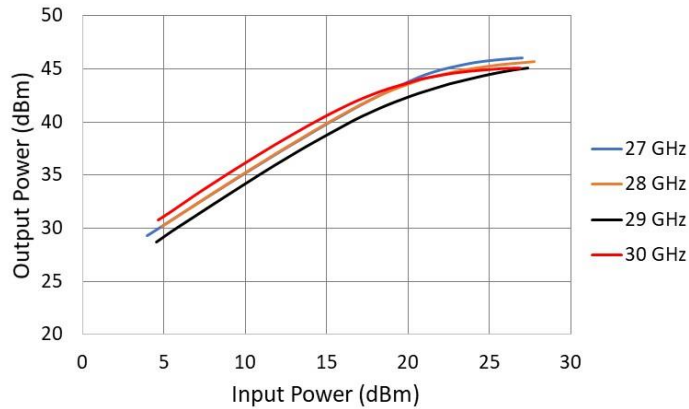
Test Condition: $V_d = 24\text{ V}$, $I_{dq} = 2.0\text{ A}$, $P_{in} = 26\text{ dBm}$ (P_{sat})
 (CW Performance in Fixture, Typical Performance at 25°C)



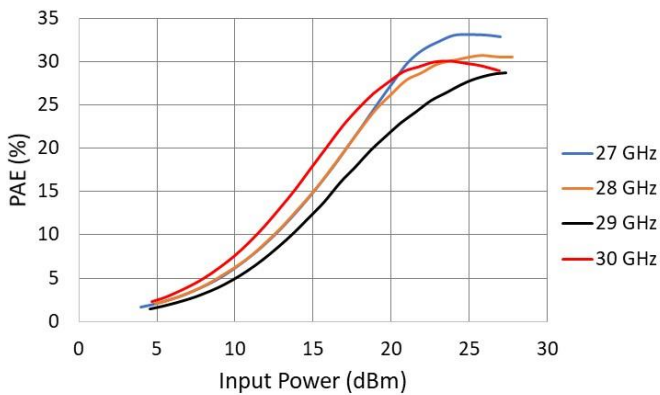
Large Signal Performance

Test Condition: $V_d = 24\text{ V}$, $I_{dq} = 2.0\text{ A}$,
 (CW Performance in Fixture, Typical Performance at 25°C)

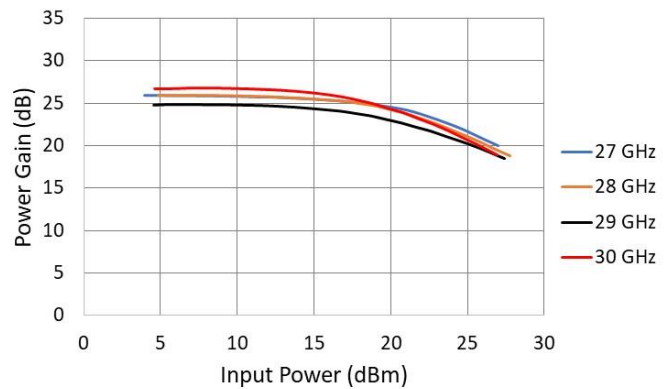
Output Power vs. Input Power vs. Frequency



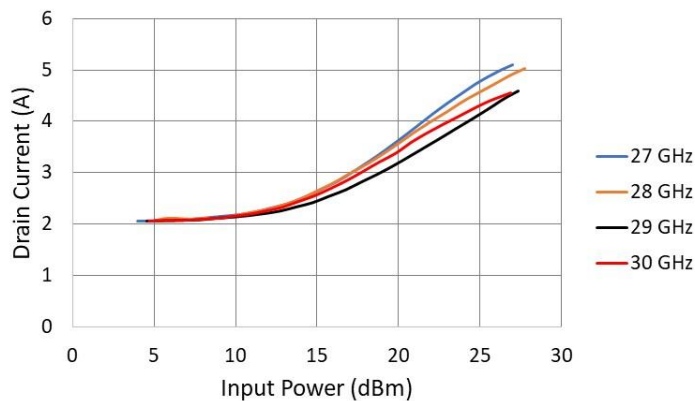
PAE vs. Input Power vs. Frequency



Power Gain vs. Input Power vs. Frequency



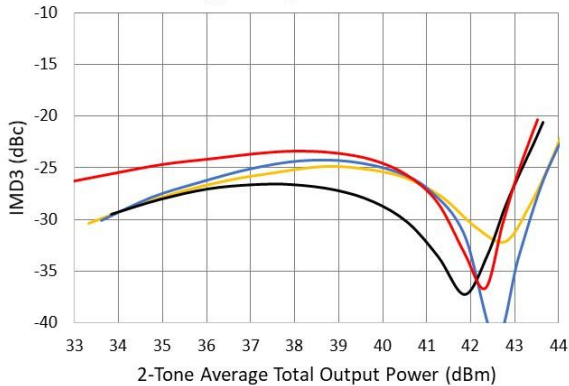
Drain Current vs. Input Power vs. Frequency



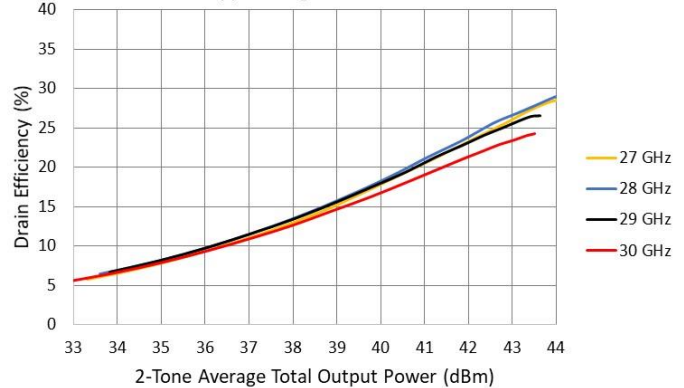
2-Tone Linearity Performance

10 MHz Tone Spacing , CW Performance in Fixture, Typical Performance at 25°C,
Bias as Indicated in Figure

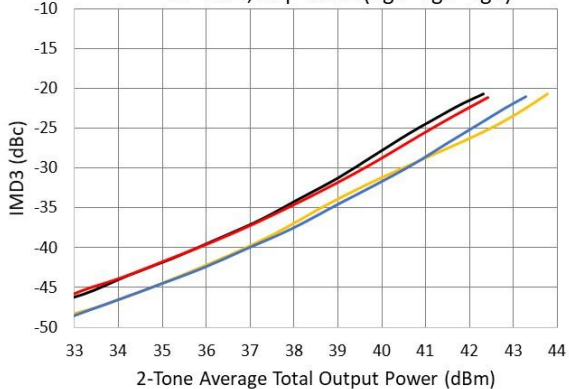
IMD3 vs. 2-Tone Output Power vs. Frequency
Vd = 26 V, Idq per stage = 0.285, 0.070, 0.860 A



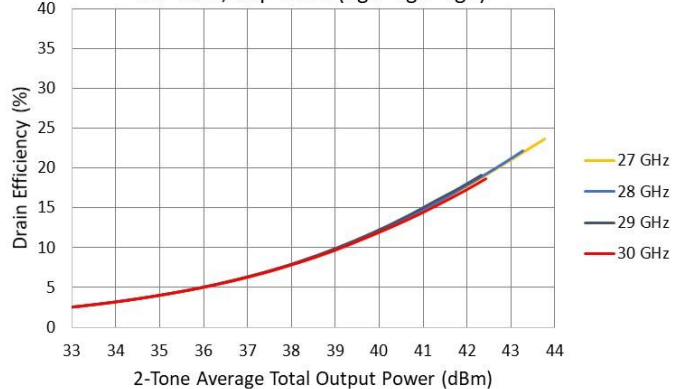
Drain Efficiency vs. 2-Tone Output Power vs. Frequency
Vd = 26 V, Idq per stage = 0.285, 0.070, 0.860 A



IMD3 vs. 2-Tone Output Power vs. Frequency
Vd = 26 V, Idq = 3.0 A (Vg1=Vg2=Vg3)



Drain Efficiency vs. 2-Tone Output Power vs. Frequency
Vd = 26 V, Idq = 3.0 A (Vg1=Vg2=Vg3)



Thermal Information

RF = Off

Parameter	Condition	Value	Unit
Thermal Resistance ($R_{\theta JC}$)	RF=OFF	1.24	°C/W
Junction Temperature (T_j)	$T_{backside}=85\text{ °C}$, $V_d=24\text{ V}$, $I_{dq}=2.0\text{ A}$, $P_{dis}=48\text{ W}$	144.3	°C

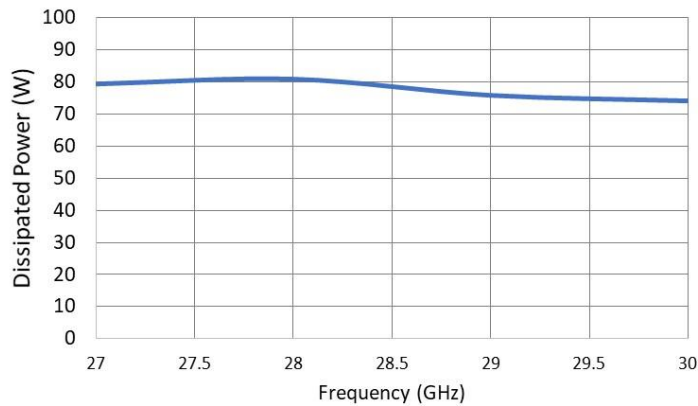
RF = On, Peak Junction Temperature at Pin = 26 dBm, Psat

Parameter	Condition	Value	Unit
Thermal Resistance ($R_{\theta JC}$)	$P_{in}=24\text{ dBm}$, Freq.=28 GHz	1.31	°C/W
Junction Temperature (T_j)	$T_{backside}=85\text{ °C}$, $V_d=24\text{ V}$, $I_d=4.8\text{ A}$, $P_{dis}=80.6\text{ W}$	190.8	°C

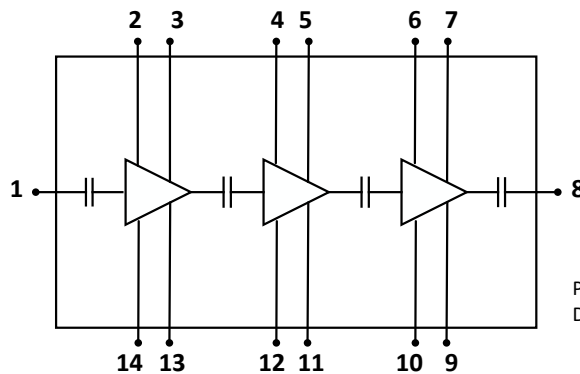
Note 1: Thermal resistance determined to the back of the chip.

Note 2: Mean time to failure per junction temperature information can be found in the following document:
[Nxbeam_GaN20MMIC_Reliability.pdf](#)

Dissipated Power vs. Frequency (at 26 dBm Pin)



Circuit Block Diagram



Pin number information detailed under Die Size and Bond Pad Information

Die Size and Bond Pad Information

Chip Size = 5000 ±25 μm x 4000 ±25 μm

Chip Thickness = 100 μm

Chip Backside metal is ground

RF Input/Output Pad Dimensions = 134 μm x 208 μm

DC Pad Dimensions:

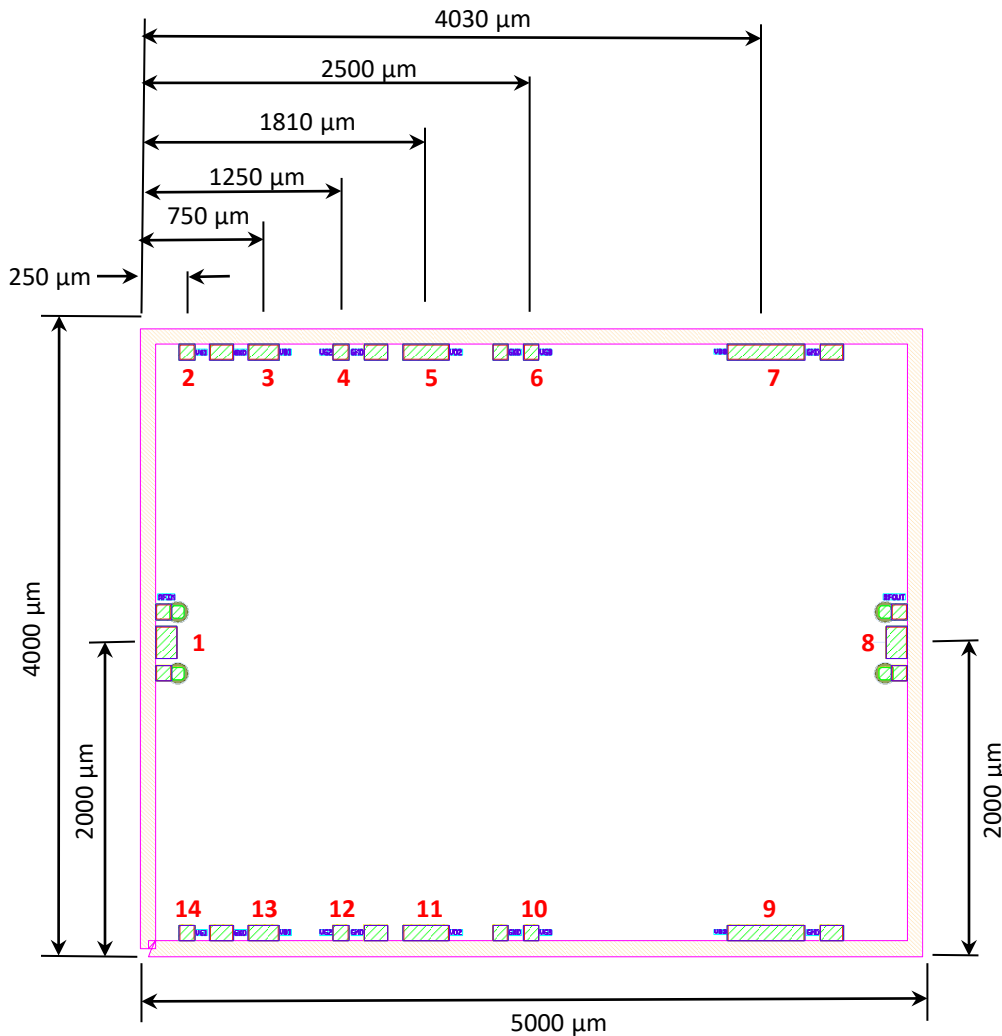
Vg1, Vg2, Vg3 = 100 μm x 100 μm

Vd1 = 200 μm x 100 μm

Vd2 = 300 μm x 100 μm

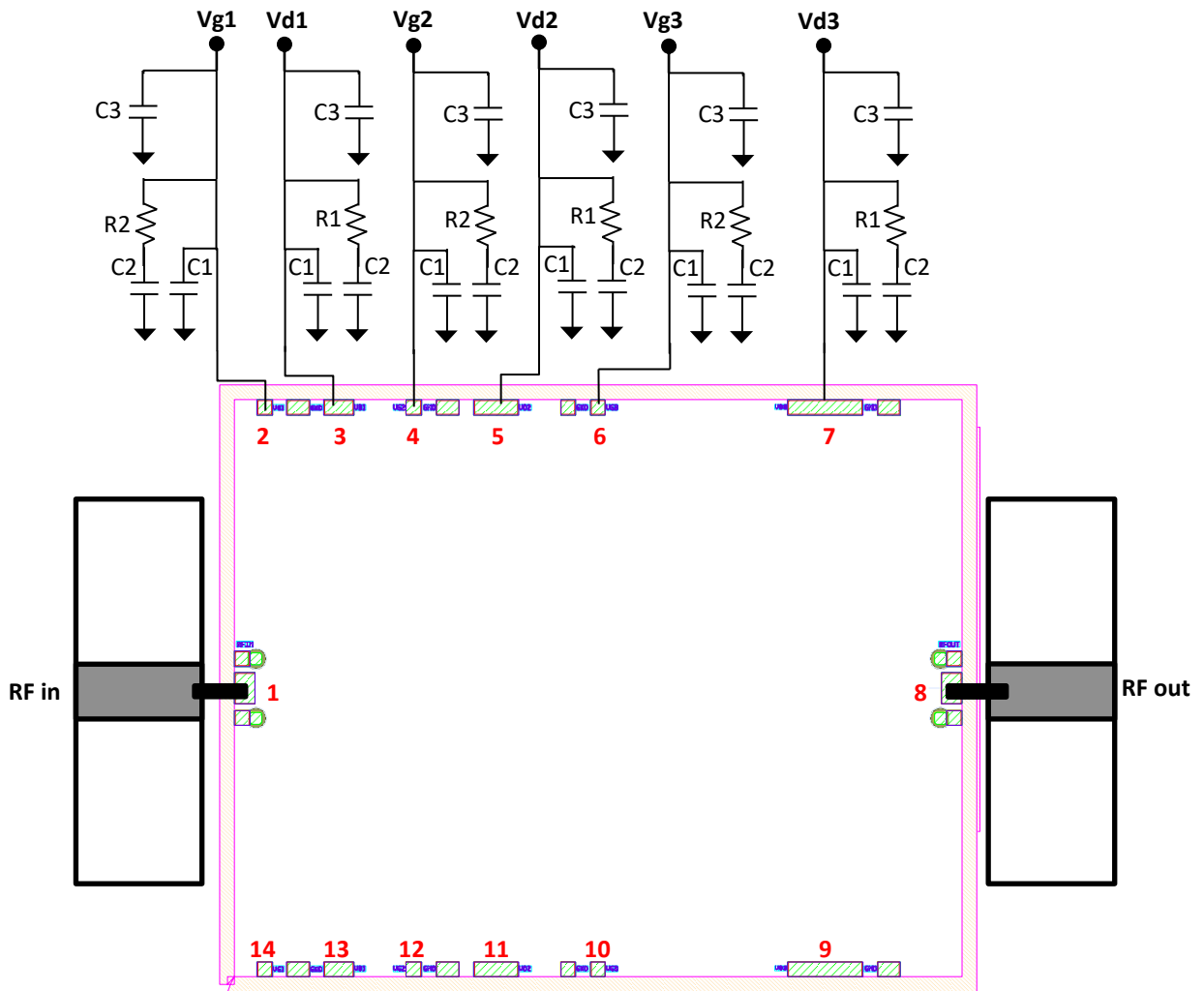
Vd3 = 500 μm x 100 μm

Pad Num.	Function
1	RF in
2, 14	Vg1
3, 13	Vd1
4, 12	Vg2
5, 11	Vd2
6, 10	Vg3
7, 9	Vd3
8	RF out



Suggested Off-Chip Components

The following diagram shows the recommended off-chip components. Bias must be applied from both sides of the chip for all drain connections and Vg3. The connection for Vg1 and Vg2 can be applied from either top or bottom. The off-chip components should be duplicated on the bottom side of the chip for connections required on both sides. All drain connections can be tied together to one source. All gate connections can be tied together to one source if desired.



Off-Chip Component Values

Capacitor	Value
C1	100 pF
C2	0.01 μ F
C3	10 μ F

Resistor	Value
R1	1 Ω
R2	10 Ω

Assembly Process

- This product has gold backside metallization and can be mounted using either a high thermal conductive epoxy or AuSn eutectic die attachment.
- Nxbeam recommends the use of AuSn eutectic die attachment due to the high-power level of this product
- Maximum recommended temperature during die attachment is 320 °C for not more than 30 seconds.
- This product contains metal air bridges so caution should be taken when handling the die to avoid damage.

Bias Information

Bias-up Procedure:

- 1.) It is recommended that voltage and current limits are set on the voltage supply's prior to biasing the product.
- 2.) Ensure power supplies are properly grounded to the product test fixture.
- 3.) Apply a negative gate voltage of -6V to Vg1, Vg2, and Vg3 to ensure all devices are pinched off.
- 4.) Gradually increase the drain bias voltage (Vd1, Vd2, Vd3) to the desired bias level but not to exceed the maximum voltage of 28 V.
- 5.) Gradually increase the gate voltages (Vg1, Vg2, Vg3) while monitoring the drain current until the desired drain current in each stage is achieved.
- 6.) Apply RF signal.

Bias-down Procedure:

- 1.) Turn off RF signal.
- 2.) Gradually decrease Vg1, Vg2, and Vg3 down to -6 V.
- 3.) Gradually decrease the drain voltages (Vd1, Vd2, Vd3) down to 0 V.
- 4.) Gradually increase gate voltages (Vg1, Vg2, Vg3) to 0 V.
- 5.) Turn off supply voltages

ESD Sensitive Product



Important Information

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