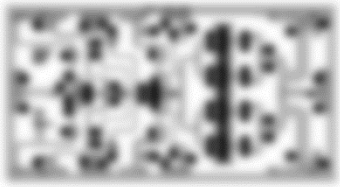
NPA2030-DE

27 – 31 GHz GaN 19 W Power Amplifier

Product Description

The Nxbeam NPA2030-DE is a Ka-band high power amplifier MMIC fabricated in 0.2um GaN HEMT on SiC. The MMIC operates from 27 to 31 GHz and provides 19 W of saturated output power, 35% average PAE, and a linear gain of 25 dB. The NPA2030-DE comes in die form with RF input and output matched to 50 Ω with DC blocking capacitors for easy system integration. The HEMT devices are fully passivated for reliable operation. Bond pad and backside metallization are Au-based for compatibility with eutectic die attachment methods.



Applications

- Ka-band Satellite Communications
- 5G Infrastructure
- Point-to-Point/Multipoint Digital Radios

Key Features

- Frequency: 27 – 31 GHz
- Linear Gain (Ave.): 25 dB
- Psat (Ave.): 19 W
- PAE (Ave.): 35%
- Chip Dimensions: 4.4 x 2.3 x 0.1 mm

Electrical Specifications

Test Condition: Vd = 24 V, Idq = 1.0 A, CW Performance in Fixture, Typical Performance at 25°C

Parameter		Min	Typical	Max	Unit
Frequency		27		31	GHz
Gain (Small Signal)	27 GHz		25.3		dB
	29 GHz		26.2		
	31 GHz		24.5		
Output Power (at Psat, Pin=22 dBm)	27 GHz		43.2		dBm
	29 GHz		42.9		
	31 GHz		42.1		
PAE (at Psat, Pin=22 dBm)	27 GHz		39.2		%
	29 GHz		35.2		
	31 GHz		34.1		
Power Gain (at Psat, Pin=22 dBm)	27 GHz		21.1		dB
	29 GHz		20.8		
	31 GHz		20.4		
Input Return Loss	27 GHz		16		dB
	29 GHz		13		
	31 GHz		20		
Output Return Loss	27 GHz		10		dB
	29 GHz		16		
	31 GHz		10		

Absolute Maximum Ratings (Temp. = 25°C)

Parameter	Min	Max	Unit
Drain Voltage (Vd1, Vd2, Vd3)		28	V
Drain Current (Id1)		300	mA
Drain Current (Id2)		720	mA
Drain Current (Id3)		2880	mA
Gate Voltage (Vg1, Vg2, Vg3)	-8	0	V
Input Power (Pin)		TBD	dBm

Recommended Operating Condition

Parameter	Value	Unit
Drain Voltage (Vd)	20 - 28	V
Drain Current (Idq)	up to 1.5	A
Gate Voltage (Vg) (Typical)	-4.1	V

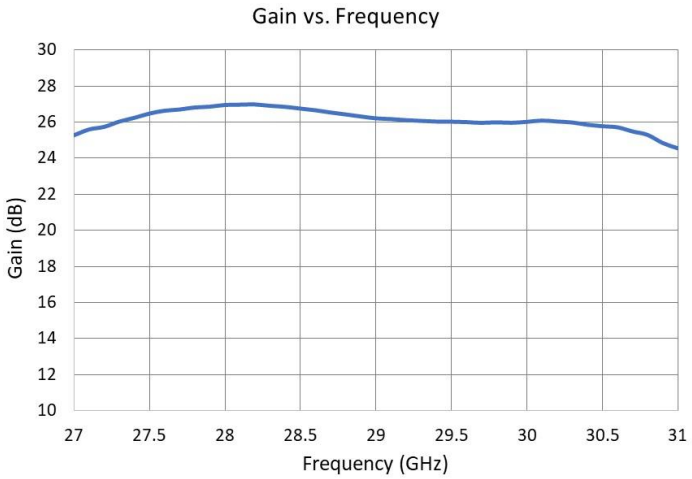
5151 Oceanus Dr., Suite 105
Huntington Beach, CA 92649

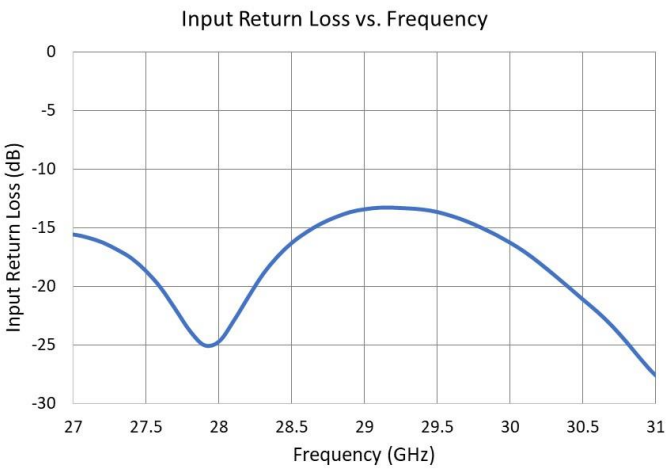
www.nxbeam.com
info@nxbeam.com

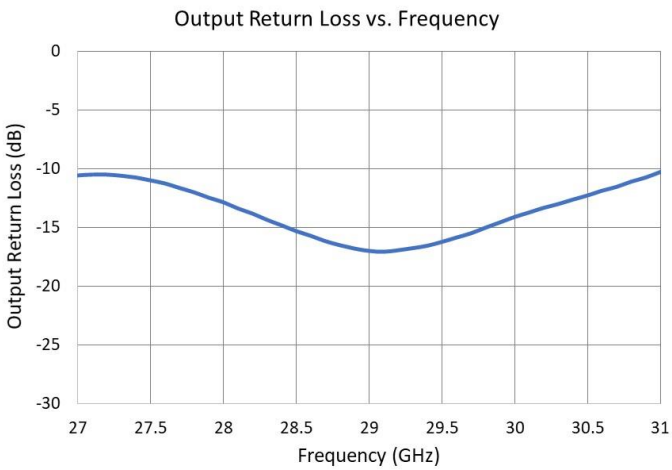
Phone: 949-656-2883

Small Signal Performance

Test Condition: Vd = 24 V, Idq = 1.0 A, (CW Performance in Fixture, Typical Performance at 25°C)







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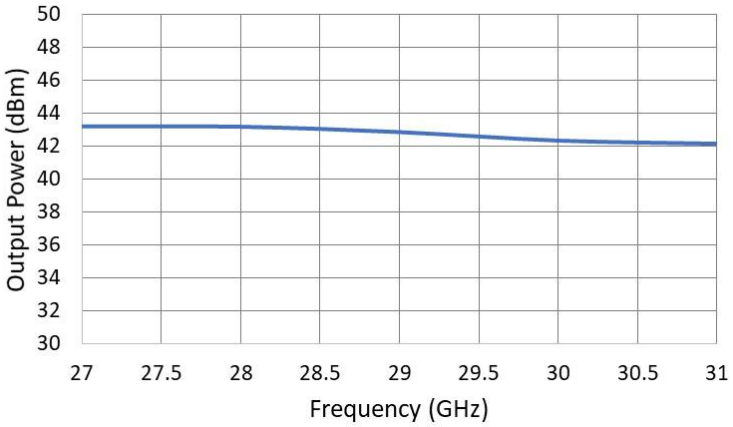
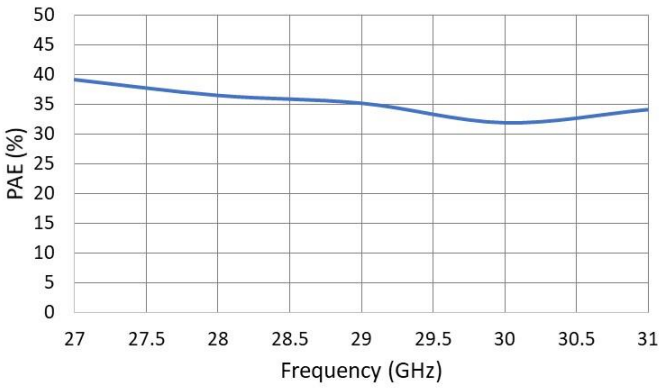
Large Signal Performance

Test Condition: Vd = 24 V, Idq = 1.0 A, Pin = 22 dBm (Psat)
(CW Performance in Fixture, Typical Performance at 25°C)

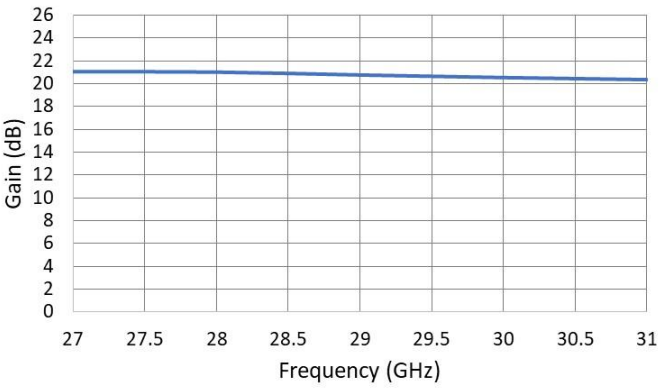
Output Power vs. Frequency (at 22 dBm Pin)



PAE vs. Frequency (at 22 dBm Pin)



Gain vs. Frequency (at 22 dBm Pin)



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Huntington Beach, CA 92649
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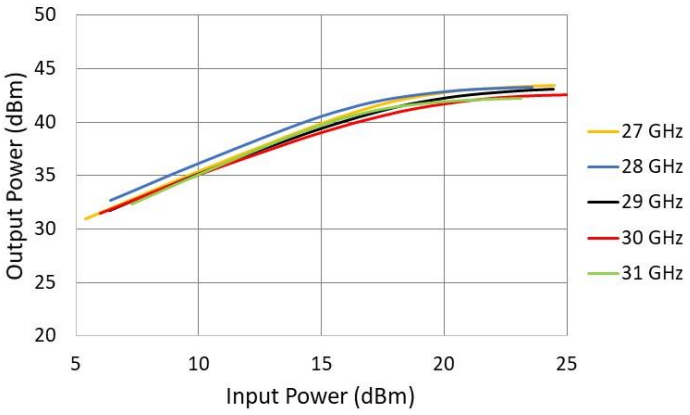
info@nxbeam.com
Phone: 949-656-2883

Large Signal Performance

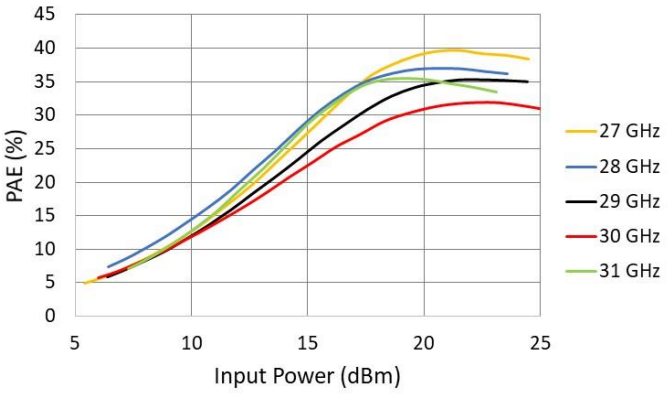
Test Condition: Vd = 24 V, Idq = 1.0 A

(CW Performance in Fixture, Typical Performance at 25°C)

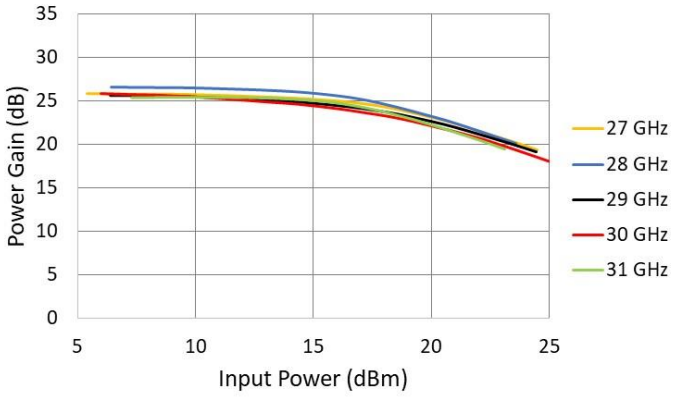
Output Power vs. Input Power vs. Frequency



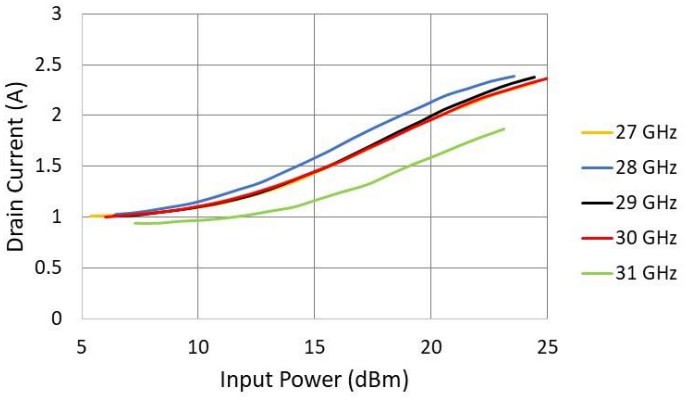
PAE vs. Input Power vs. Frequency



Power Gain vs. Input Power vs. Frequency



Drain Current vs. Input Power vs. Frequency



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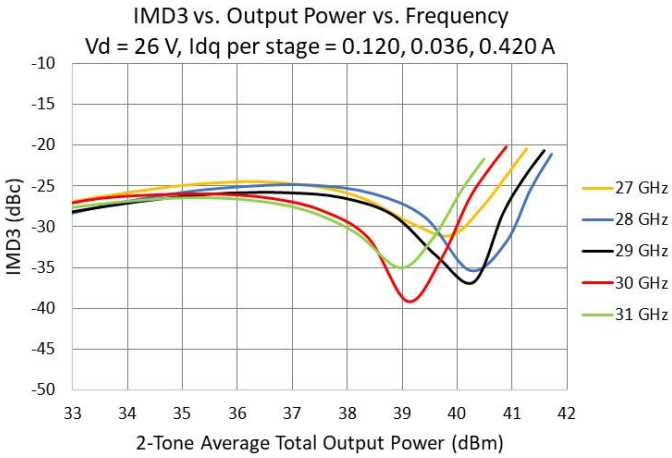
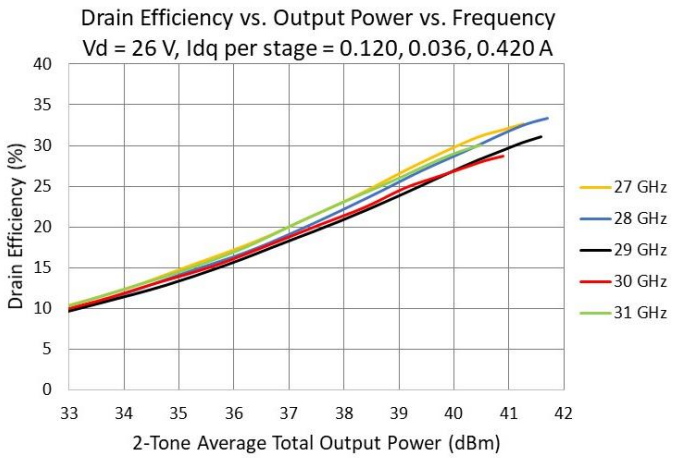
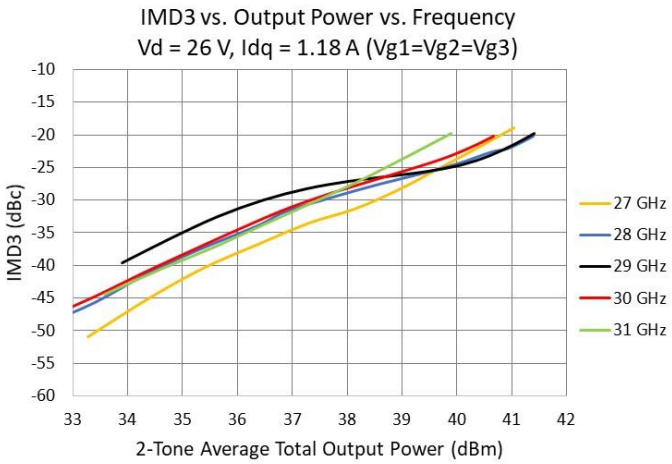
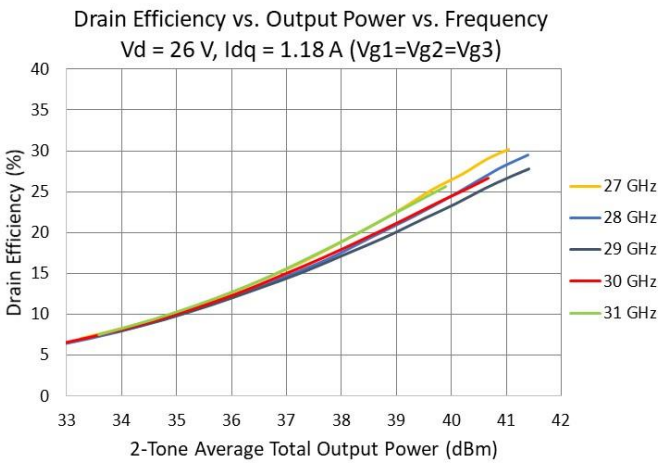
2-Tone Linearity Performance

10 MHz Tone Spacing , CW Performance in Fixture, Typical Performance at 25°C,









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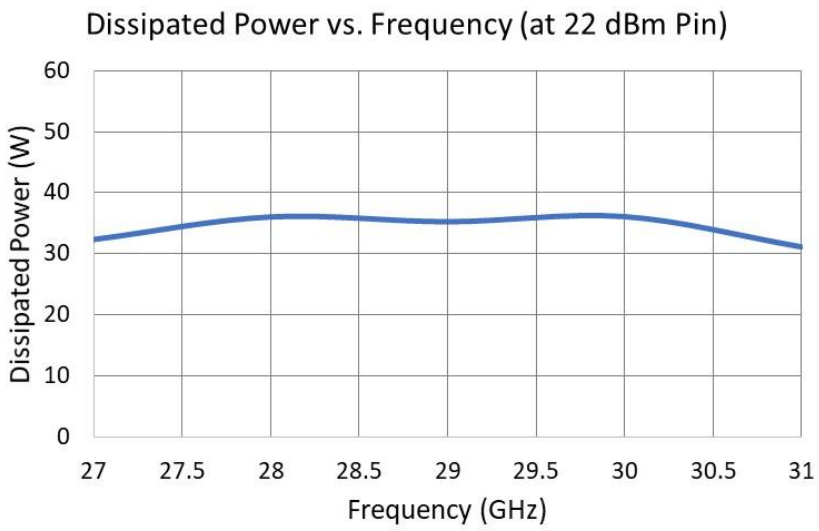
Thermal Information

RF = Off

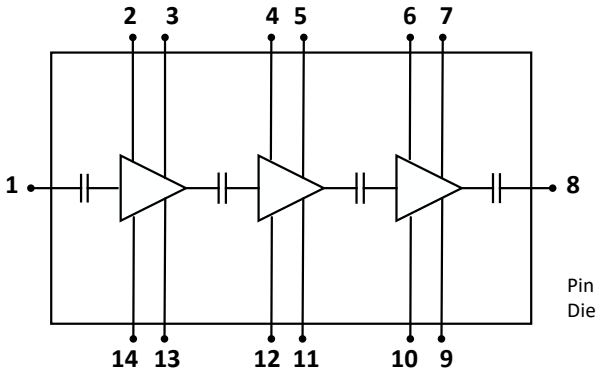
Parameter	Condition	Value	Unit
Thermal Resistance ($R_{\Theta JC}$)	RF=OFF	2.5	°C/W
Junction Temperature (Tj)	$T_{backside}$=85 °C, V_d=24 V, I_{dq}=1.0 A, P_{dis}=24 W	144.8	°C

RF = On, Peak Junction Temperature at Pin = 21 dBm, Psat

Parameter	Condition	Value	Unit
Thermal Resistance ($R_{\Theta JC}$)	P_{in}=22 dBm, Freq.=30 GHz	2.6	°C/W
Junction Temperature (Tj)	$T_{backside}$=85 °C, V_d=24 V, I_d=2.21 A, P_{dis}=36.1 W	179.3	°C



Circuit Block Diagram



Pin number information detailed under Die Size and Bond Pad Information

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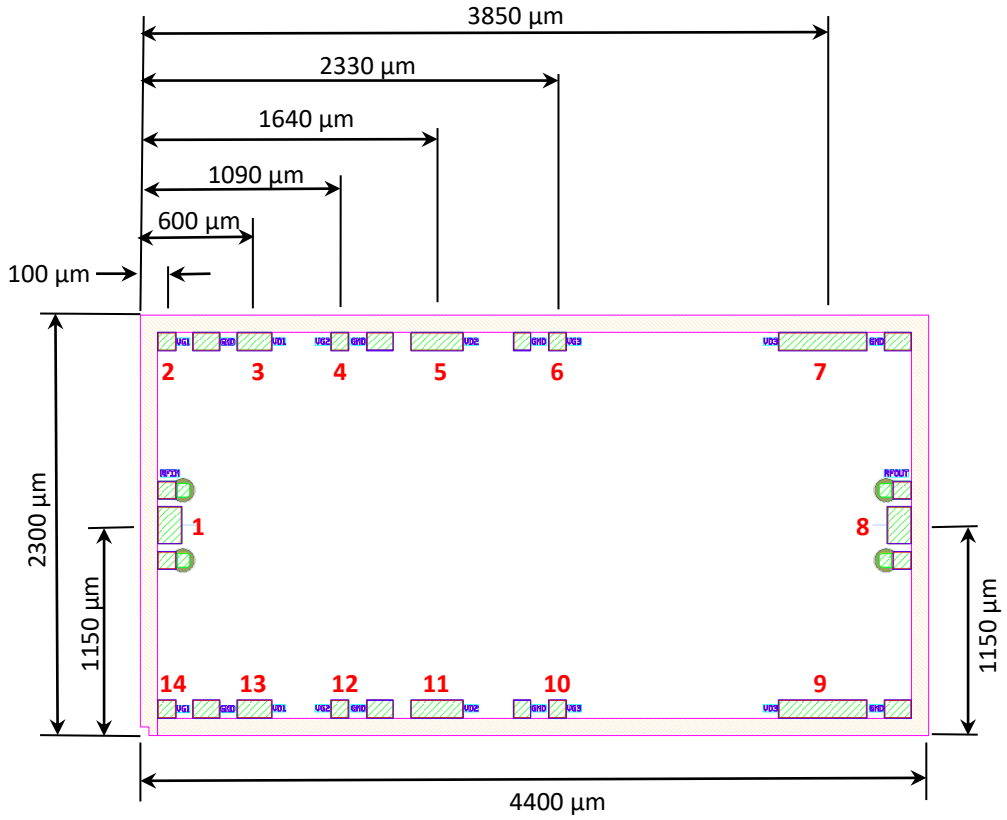
Die Size and Bond Pad Information

Chip Size = 4400 ±25 um x 2300 ±25 um
Chip Thickness = 100 um
Chip Backside metal is ground

RF Input/Output Pad Dimensions = 134 um x 208 um
DC Pad Dimensions:
- Vg1, Vg2, Vg3 = 100 um x 100 um
- Vd1 = 200 um x 100 um
- Vd2 = 300 um x 100 um
- Vd3 = 500 um x 100 um

Pad Num.	Function
1	RF in
2, 14	Vg1
3, 13	Vd1
4, 12	Vg2
5, 11	Vd2
6, 10	Vg3
7, 9	Vd3
8	RF out



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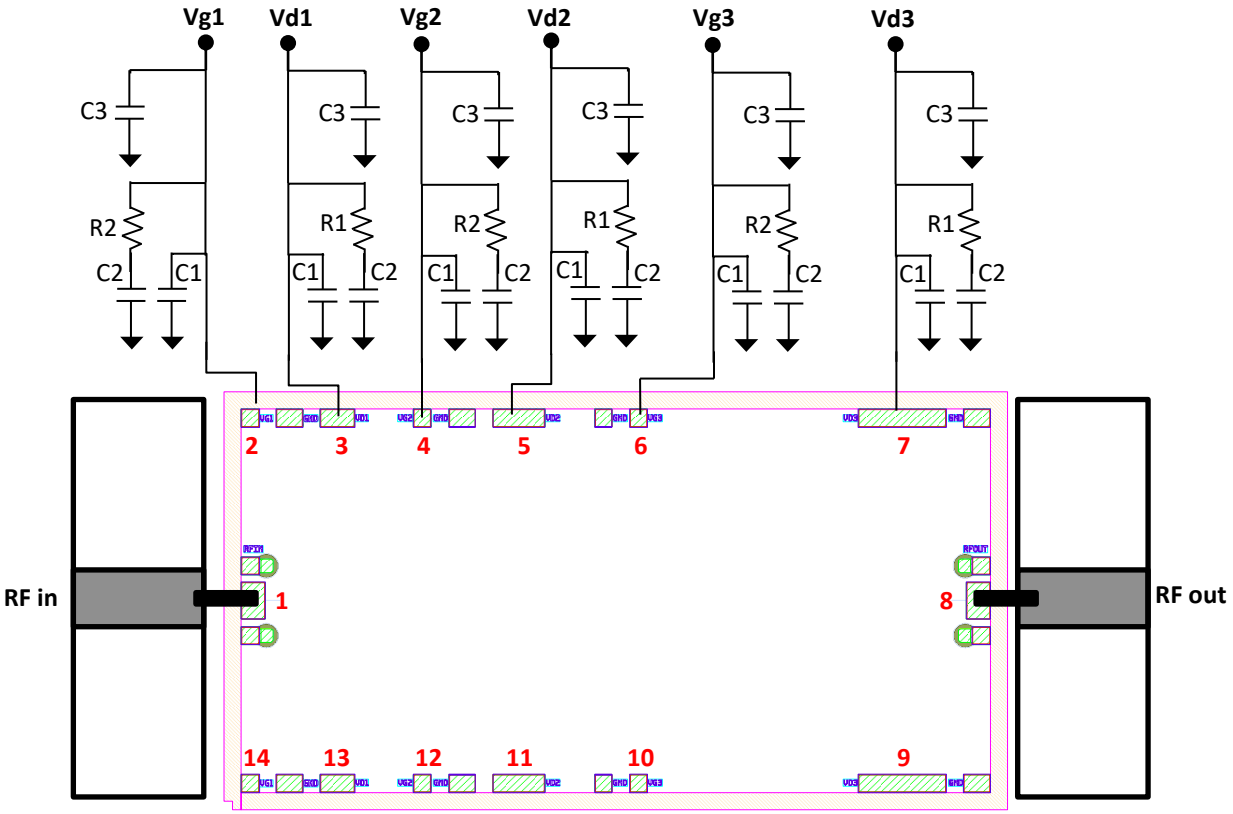
Suggested Off-Chip Components

The following diagram is a suggested bonding arraignment with off-chip components. All drain connections can be tied together to one source. All gate connections can be tied together to one source if desired. The NPA2030-DE can be biased from either top or bottom of the chip as well as from both sides if desired.



Off-Chip Component Values

Capacitor	Value
C1	100 pF
C2	0.01 µF
C3	1 µF

Resistor	Value
R1	1 Ω
R2	10 Ω

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Assembly Process

- This product has gold backside metallization and can be mounted using either a high thermal conductive epoxy or AuSn eutectic die attachment.
- Nxbeam recommends the use of AuSn eutectic die attachment due to the high-power level of this product
- Maximum recommended temperature during die attachment is 320 °C for not more than 30 seconds.
- This product contains metal air bridges so caution should be taken when handling the die to avoid damage.

Bias Information

The NPA2030-DE can be biased from either top or bottom of the chip as well as from both sides if desired.

Bias-up Procedure:

1.) It is recommended that voltage and current limits are set on the voltage supply's prior to biasing the product.
2.) Ensure power supplies are properly grounded to the product test fixture.
3.) Apply a negative gate voltage of -6V to Vg1, Vg2, and Vg3 to ensure all devices are pinched off.
4.) Gradually increase the drain bias voltage (Vd1, Vd2, Vd3) to the desired bias level but not to exceed the maximum voltage of 28 V.
5.) Gradually increase the gate voltages (Vg1, Vg2, Vg3) while monitoring the drain current until the desired drain current in each stage is achieved.
6.) Apply RF signal.

Bias-down Procedure:

1.) Turn off RF signal.
2.) Gradually decrease Vg1, Vg2, and Vg3 down to -6 V.
3.) Gradually decrease the drain voltages (Vd1, Vd2, Vd3) down to 0 V.
4.) Gradually increase gate voltages (Vg1, Vg2, Vg3) to 0 V.
5.) Turn off supply voltages

ESD Sensitive Product

Important Information

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