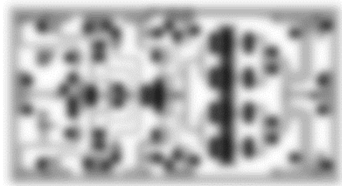
Nxbeam™

NPA2030-DE

27.5 – 31 GHz GaN 20 W Power Amplifier

Product Description

The Nxbeam NPA2030-DE is a Ka-band high power amplifier MMIC fabricated in 0.2um GaN HEMT on SiC. The MMIC operates from 27.5 to 31 GHz and provides 20 W of saturated output power, 35% average PAE, and a linear gain of 25 dB. The NPA2030-DE comes in die form with RF input and output matched to 50 Ω with DC blocking capacitors for easy system integration. The HEMT devices are fully passivated for reliable operation. Bond pad and backside metallization are Au-based for compatibility with eutectic die attachment methods.



Applications

- Ka-band Satellite Communications
- 5G Infrastructure
- Point-to-Point/Multipoint Digital Radios

Key Features

- Frequency: 27.5 – 31 GHz
- Linear Gain (Ave.): 25 dB
- Psat (Ave.): 20 W
- PAE (Ave.): 35%
- Chip Dimensions: 4.375 x 2.275 x 0.1 mm

Electrical Specifications

Test Condition: Vd = 24 V, Idq = 1.0 A, CW Performance in Fixture, Typical Performance at 25°C

Parameter		Min	Typical	Max	Unit
Frequency		27.5		31	GHz
Gain (Small Signal)	27.5 GHz		25.4		dB
	29 GHz		25.2		
	31 GHz		23.5		
Output Power (at Psat, Pin=22 dBm)	27.5 GHz		43.2		dBm
	29 GHz		42.9		
	31 GHz		42.1		
PAE (at Psat, Pin=22 dBm)	27.5 GHz		36.5		%
	29 GHz		35.2		
	31 GHz		34.1		
Power Gain (at Psat, Pin=22 dBm)	27.5 GHz		21		dB
	29 GHz		20.8		
	31 GHz		20.4		
Input Return Loss	27.5 GHz		18		dB
	29 GHz		13		
	31 GHz		20		
Output Return Loss	27.5 GHz		11		dB
	29 GHz		16		
	31 GHz		10		

Maximum Quiescent Bias

Parameter	Max	Unit
Drain Voltage (Vd1, Vd2, Vd3)	28	V
Drain Current (Id1)	120	mA
Drain Current (Id2)	285	mA
Drain Current (Id3)	1150	mA

Maximum quiescent bias represents the operational bias used during reliability life testing. Biasing the part at or below this bias ensures reliability will be bound by the published reliability results.

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Absolute Maximum Ratings (Temp. = 25°C)

Parameter	Min	Max	Unit
Drain Voltage (Vd1, Vd2, Vd3)		28	V
Drain Current (Id1)		300	mA
Drain Current (Id2)		720	mA
Drain Current (Id3)		2880	mA
Gate Voltage (Vg1, Vg2, Vg3)	-8	0	V

Absolute maximum ratings represent the maximum current under power saturation conditions.

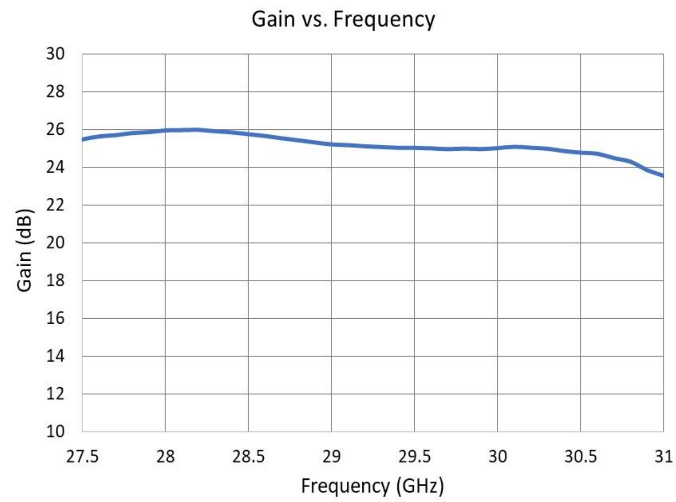
Recommended Quiescent Operating Condition

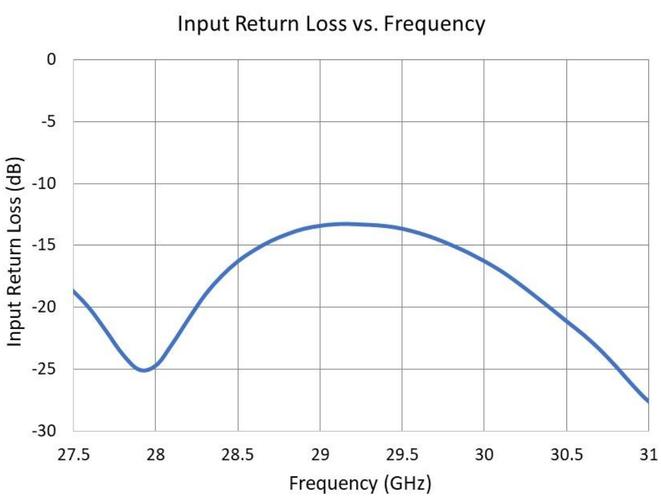
Parameter	Max	Unit
Drain Voltage (Vd1, Vd2, Vd3)	20 - 28	V
Drain Current (Id1)	up to 120	mA
Drain Current (Id2)	up to 285	mA
Drain Current (Id3)	up to 1150	mA
Gate Voltage (typical range)	-6 to -3.5	0

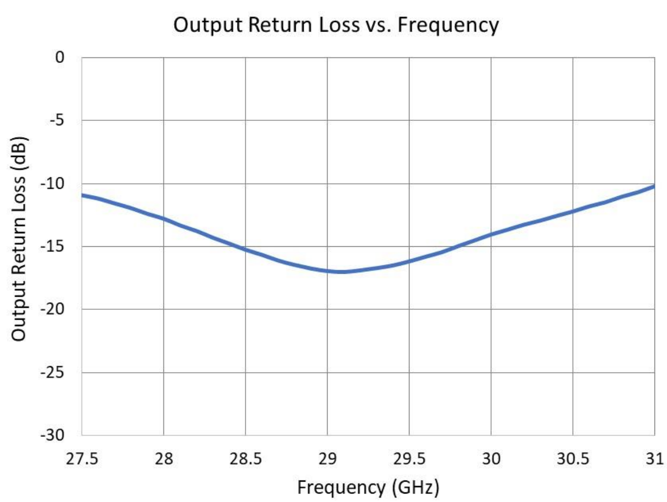
Gate voltage will vary based on desired current per stage

Small Signal Performance

Test Condition: Vd = 24 V, Idq = 1.0 A, (CW Performance in Fixture, Typical Performance at 25°C)







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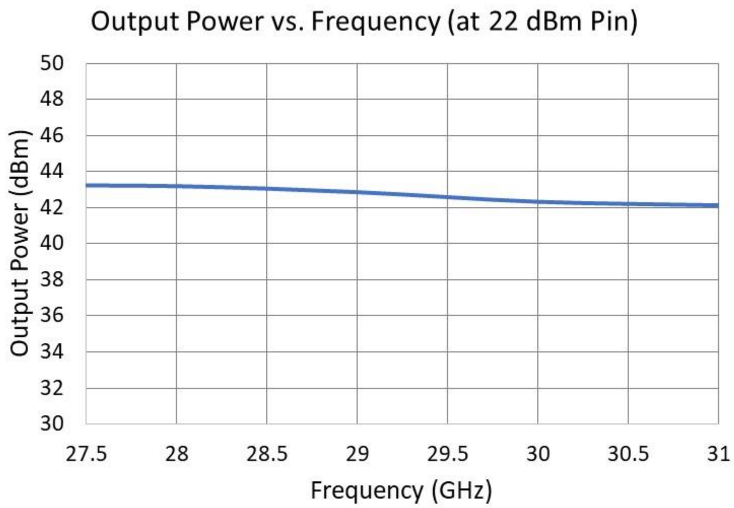
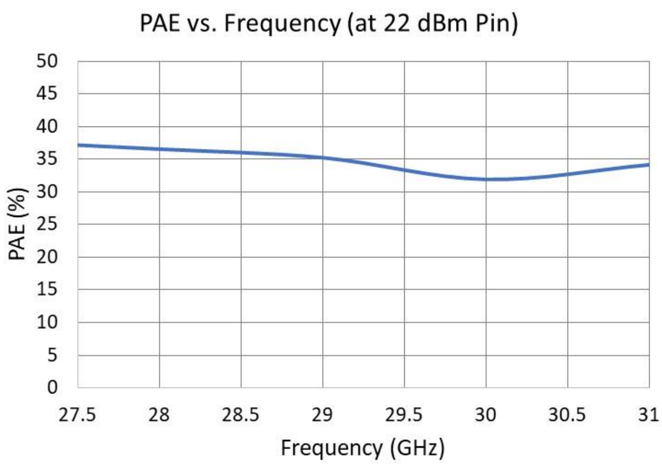
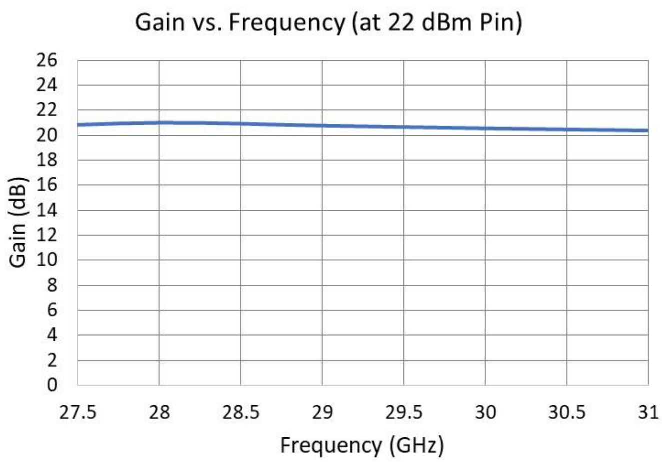
Large Signal Performance

Test Condition: Vd = 24 V, Idq = 1.0 A, Pin = 22 dBm (Psat)
(CW Performance in Fixture, Typical Performance at 25°C)







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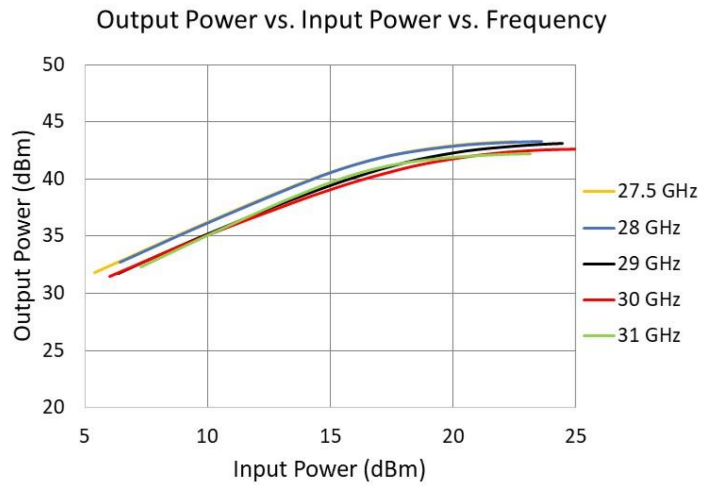
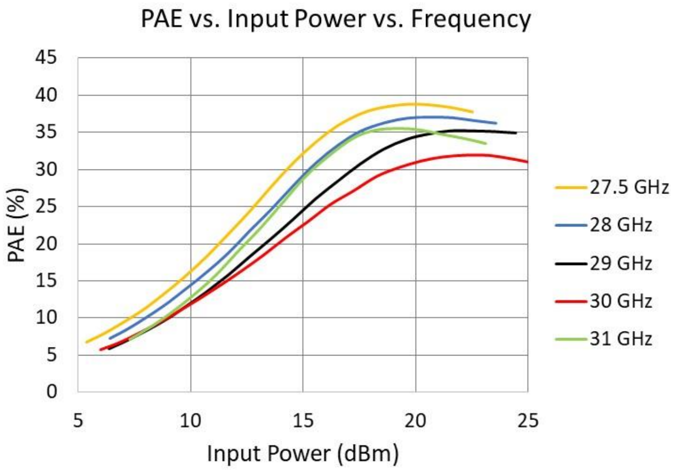
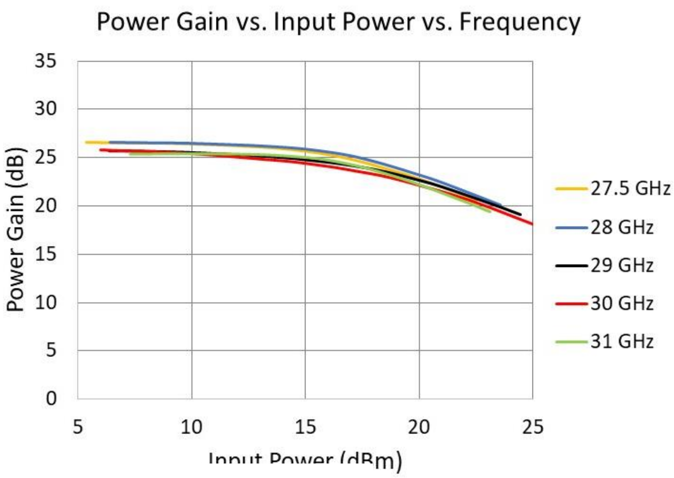
Large Signal Performance

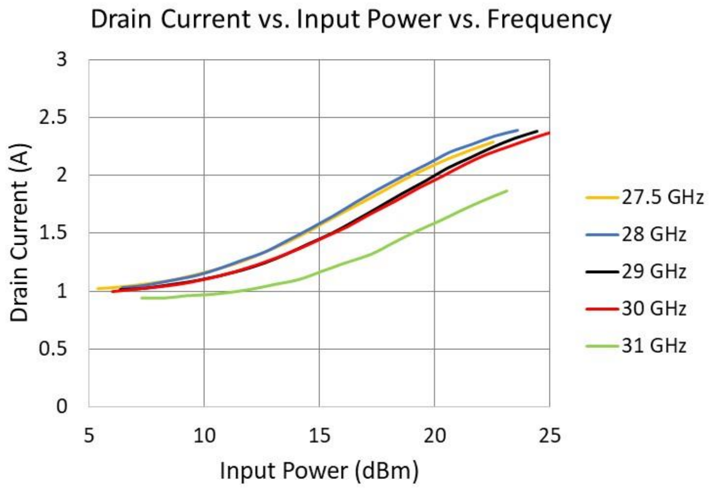
Test Condition: Vd = 24 V, Idq = 1.0 A

(CW Performance in Fixture, Typical Performance at 25°C)









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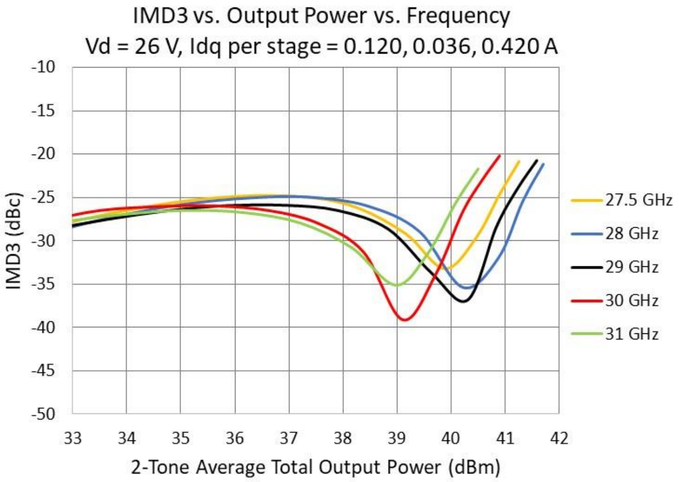
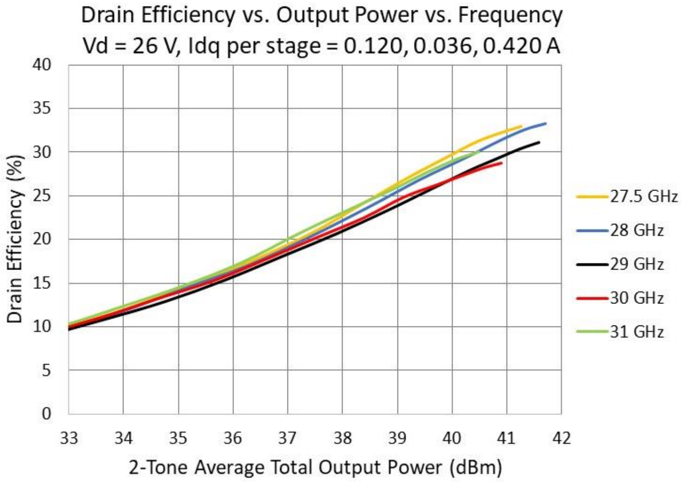
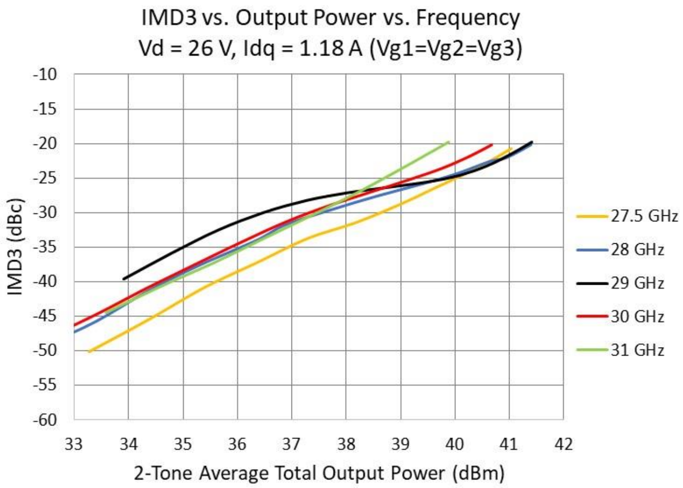
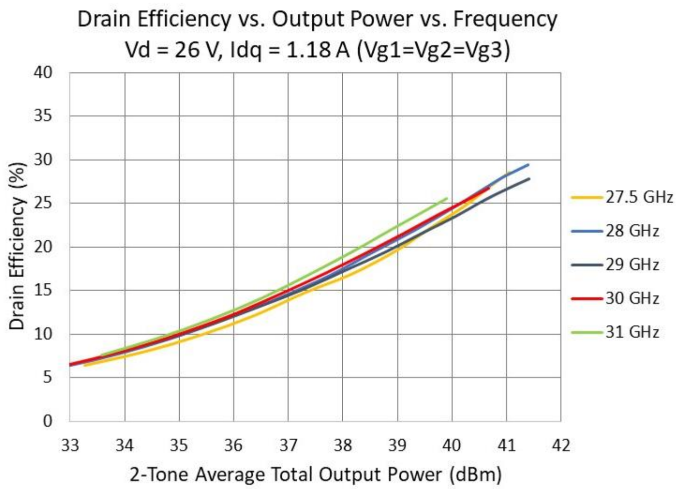
2-Tone Linearity Performance

10 MHz Tone Spacing , CW Performance in Fixture, Typical Performance at 25°C,









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Thermal Information

RF = Off

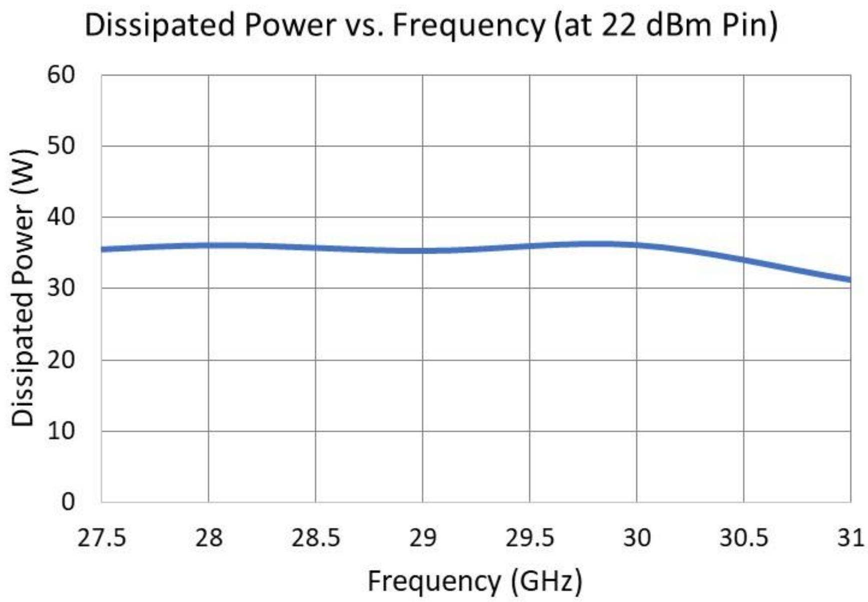
Parameter	Condition	Value	Unit
Thermal Resistance ($R_{\Theta JC}$)	RF=OFF	2.5	°C/W
Junction Temperature (Tj)	$T_{backside}$=85 °C, V_d=24 V, I_{dq}=1.0 A, P_{dis}=24 W	144.8	°C

RF = On, Peak Junction Temperature at Pin = 21 dBm, Psat

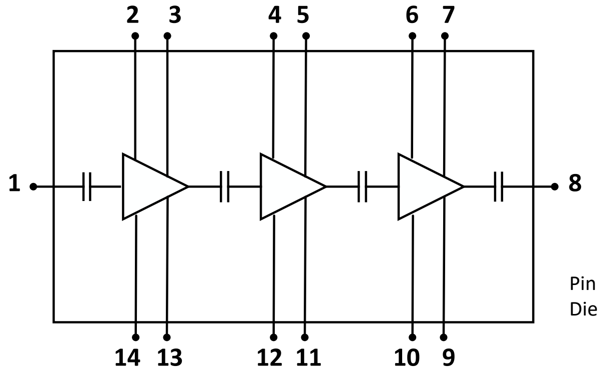
Parameter	Condition	Value	Unit
Thermal Resistance ($R_{\Theta JC}$)	P_{in}=22 dBm, Freq.=30 GHz	2.6	°C/W
Junction Temperature (Tj)	$T_{backside}$=85 °C, V_d=24 V, I_d=2.21 A, P_{dis}=36.1 W	179.3	°C

Note 1: Thermal resistance determined to the back of the chip.

Note 2: Mean time to failure per junction temperature information can be found in the following document: Nxbeam_GaN20MMIC_Reliability.pdf



Circuit Block Diagram



Pin number information detailed under Die Size and Bond Pad Information

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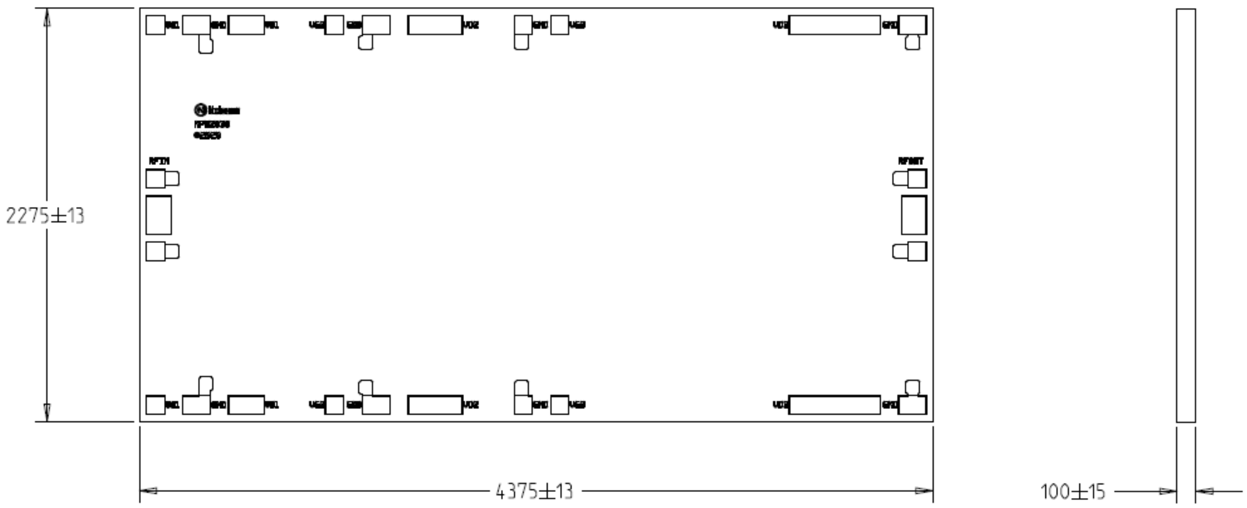
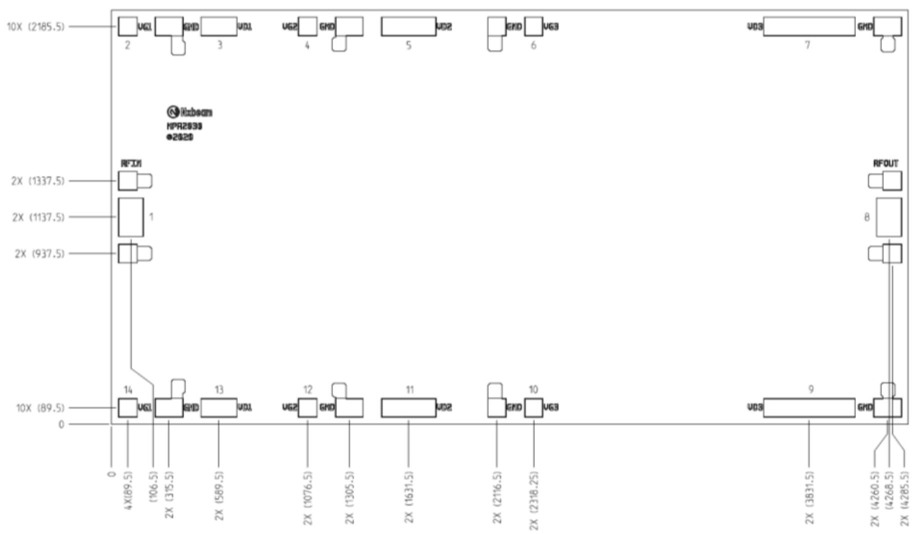
Die Size and Bond Pad Information

ID	FUNCTION	PAD NUMBER	PAD SIZE (MICRONS)
RFIN	RF INPUT	1	134 X 208
RFOUT	RF OUTPUT	8	134 X 208
VG1	GATE VOLTAGE - STAGE 1 (-8V MIN, 0V MAX)	2,14	100 X 100
VD1	DRAIN VOLTAGE - STAGE 1 (0V MIN, 28V MAX)	3,13	200 X 100
VG2	GATE VOLTAGE - STAGE 2 (-8V MIN, 0V MAX)	4,12	100 X 100
VD2	DRAIN VOLTAGE - STAGE 2 (0V MIN, 28V MAX)	5,11	300 X 100
VG3	GATE VOLTAGE - STAGE 3 (-8V MIN, 0V MAX)	6,10	100 X 100
VD3	DRAIN VOLTAGE - STAGE 3 (0V MIN, 28V MAX)	7,9	500 X 100





Chip Backside metal is ground

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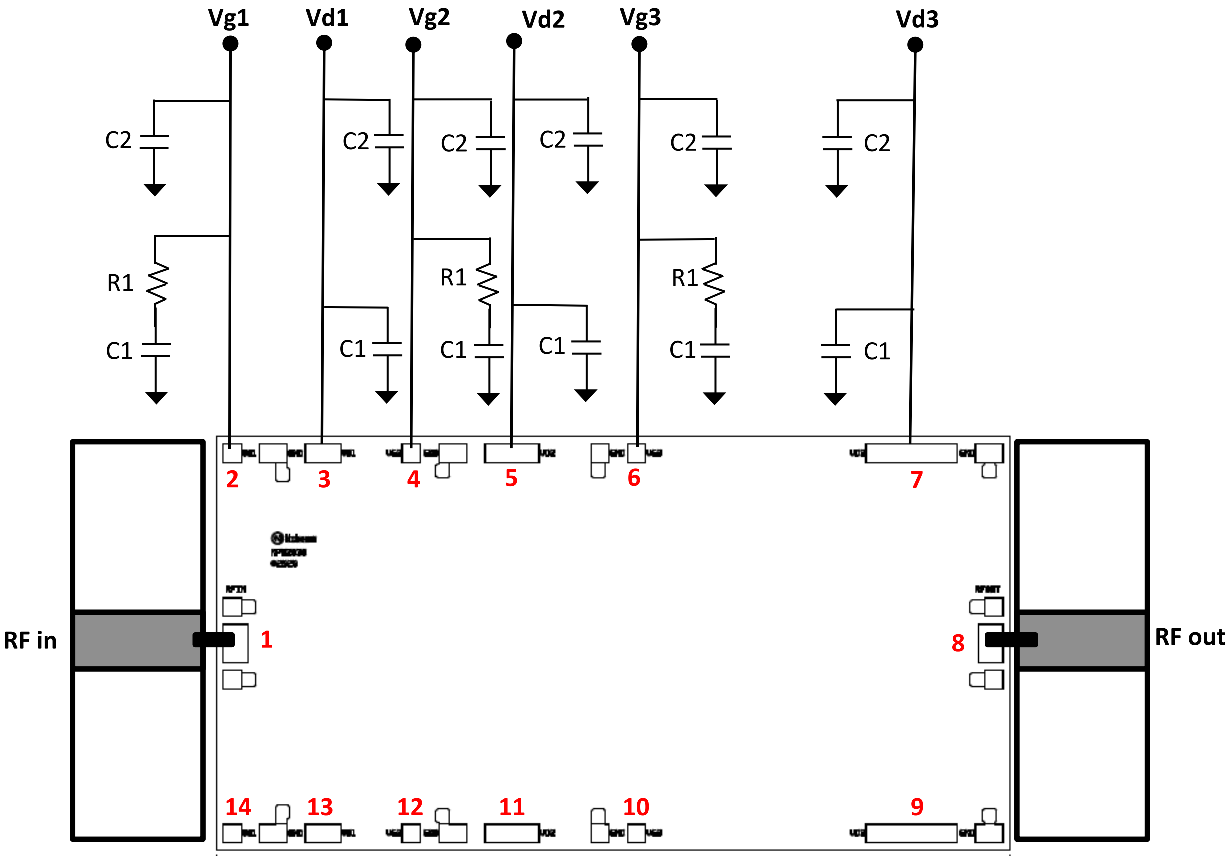
Suggested Off-Chip Components

The following diagram is a suggested bonding arraignment with off-chip components. All drain connections can be tied together to one source. All gate connections can be tied together to one source if desired. The NPA2030-DE can be biased from either top or bottom of the chip as well as from both sides if desired.



Off-Chip Component Values

Resistor	Value
R1	10 Ω

Capacitor	Value
C1	0.01 µF
C2	1 µF

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Assembly Process

- This product has gold backside metallization and can be mounted using either a high thermal conductive epoxy or AuSn eutectic die attachment.
- Nxbeam recommends the use of AuSn eutectic die attachment due to the high-power level of this product
- Maximum recommended temperature during die attachment is 320 °C for not more than 30 seconds.
- This product contains metal air bridges so caution should be taken when handling the die to avoid damage.

Bias Information

The NPA2030-DE can be biased from either top or bottom of the chip as well as from both sides if desired.

Bias-up Procedure:

1.) It is recommended that voltage and current limits are set on the voltage supply's prior to biasing the product.
2.) Ensure power supplies are properly grounded to the product test fixture.
3.) Apply a negative gate voltage of -6V to Vg1, Vg2, and Vg3 to ensure all devices are pinched off.
4.) Gradually increase the drain bias voltage (Vd1, Vd2, Vd3) to the desired bias level but not to exceed the maximum voltage of 28 V.
5.) Gradually increase the gate voltages (Vg1, Vg2, Vg3) while monitoring the drain current until the desired drain current in each stage is achieved.
6.) Apply RF signal.

Bias-down Procedure:

1.) Turn off RF signal.
2.) Gradually decrease Vg1, Vg2, and Vg3 down to -6 V.
3.) Gradually decrease the drain voltages (Vd1, Vd2, Vd3) down to 0 V.
4.) Gradually increase gate voltages (Vg1, Vg2, Vg3) to 0 V.
5.) Turn off supply voltages

ESD Sensitive Product

Export Information

This product is controlled by US law for export under the ECCN 3A001.b.2.c. The purchaser of this product, whether in the US or abroad, is responsible for compliance with all US laws regarding export, transfer, or re-transfer of this product. For more information, please refer to the Export Administration Regulations at https://www.bis.doc.gov/index.php. Nxbeam reminds you that it is your responsibility to ascertain your export compliance obligations and to comply with all applicable laws and regulations.

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