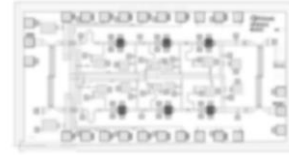


### Product Description

The Nxbeam NPA4010-DE is a V-band power amplifier MMIC fabricated in 0.15um GaN HEMT on SiC. This part is ideally suited for V-band satellite and point-to-point communications applications. The MMIC operates from 47 to 52 GHz and provides 3.5 W saturated output power, 23% PAE, and 24 dB of linear gain. The NPA4010-DE comes in die form with RF input and output matched to 50  $\Omega$  with DC blocking capacitors for easy system integration. The HEMT devices are fully passivated for reliable operation. Bond pad and backside metallization are Au-based for compatibility with eutectic die attachment methods.



### Applications

- V-band Satellite Communications
- 5G Infrastructure
- Point-to-Point/Multipoint Digital Radios

### Key Features

- Frequency: 47 – 52 GHz
- Linear Gain (Ave.): 24 dB
- Psat (Ave.): 3.5 W
- PAE (Ave.): 23%
- Chip Dimensions: 2.85 x 1.45 x 0.075 mm

### Electrical Specifications (Small Signal)

Test Condition:  $V_d = 24$  V,  $I_{dq} = 0.6$  A, Pulsed On-wafer Measurements, Typical Performance at 25°C

Parameter		Min	Typical	Max	Unit
Frequency		47		52	GHz
Gain (Small Signal)	47 GHz		20.5		dB
	49.5 GHz		26.7		
	52 GHz		21.3		
Input Return Loss	47 GHz		20		dB
	49.5 GHz		16.7		
	52 GHz		20		
Output Return Loss	47 GHz		13		dB
	49.5 GHz		23		
	52 GHz		21		

### Electrical Specifications (Large Signal)

Test Condition:  $V_d = 24$  V,  $I_{dq} = 0.3$  A, Pulsed On-wafer Measurements, Typical Performance at 25°C

Parameter		Min	Typical	Max	Unit
Frequency		47		52	GHz
Output Power (at Psat, Pin=21 dBm)	47 GHz		35.1		dBm
	49.5 GHz		36.2		
	52 GHz		35.3		
PAE (at Psat, Pin=21 dBm)	47 GHz		20.1		%
	49.5 GHz		23.8		
	52 GHz		26.2		
Power Gain (at Psat, Pin=21 dBm)	47 GHz		14.1		dB
	49.5 GHz		15.2		
	52 GHz		14.3		

### Absolute Maximum Ratings (Temp. = 25°C)

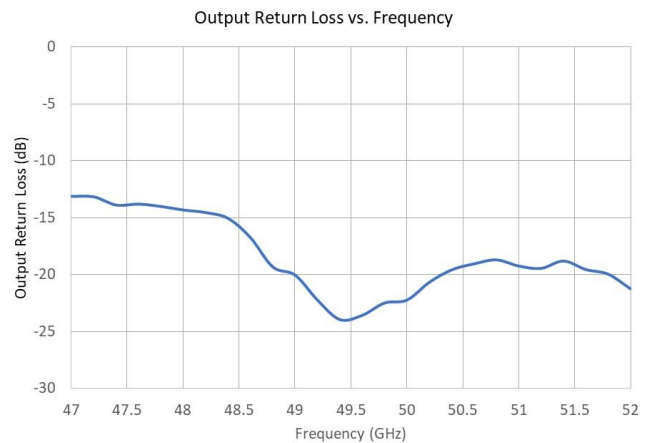
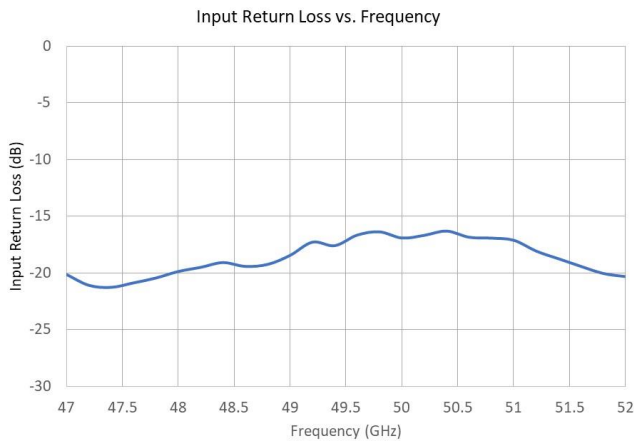
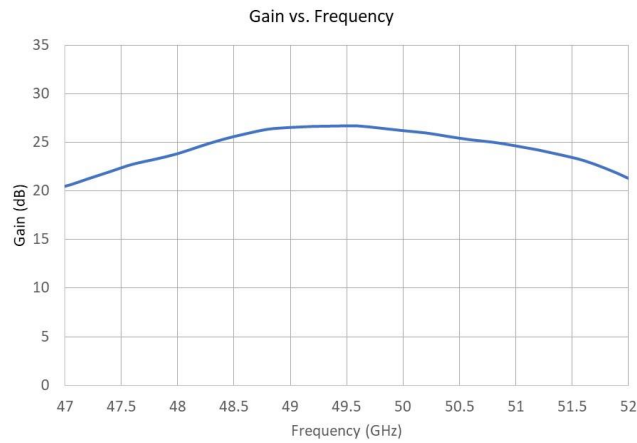
Parameter	Min	Max	Unit
Drain Voltage (Vd1)		28	V
Drain Current (Id1) from Stage 1		500	mA
Drain Current (Id1) from Stage 2		500	mA
Drain Current (Id1) from Stage 3		500	mA
Gate Voltage (Vg1, Vg2, Vg3)	-8	0	V
Input Power (Pin)		TBD	dBm

### Recommended Operating Condition

Parameter	Value	Unit
Drain Voltage (Vd)	20 - 28	V
Drain Current (Id1) from Stage 1	up to 0.2	A
Drain Current (Id1) from Stage 2	up to 0.2	A
Drain Current (Id1) from Stage 3	up to 0.2	A
Gate Voltage (Vg1, Vg2, Vg3) (Typical)	-3.8	V

### Small Signal Performance (on-wafer pulsed measurement)

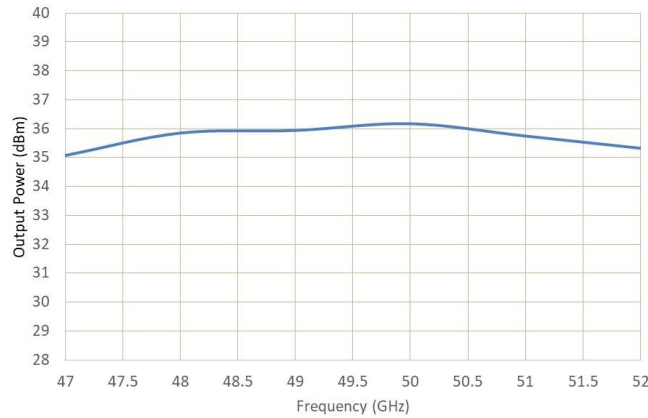
Test Condition: Vd = 24 V, Idq = 0.6 A



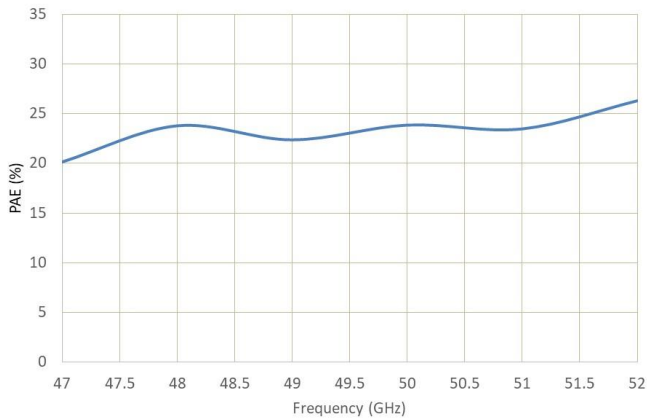
### Large Signal Performance

Test Condition:  $V_d = 24\text{ V}$ ,  $I_{dq} = 0.3\text{ A}$ ,  $P_{in} = 21\text{ dBm}$  ( $P_{sat}$ )  
 (on-wafer pulsed measurement, typical performance at 25°C)

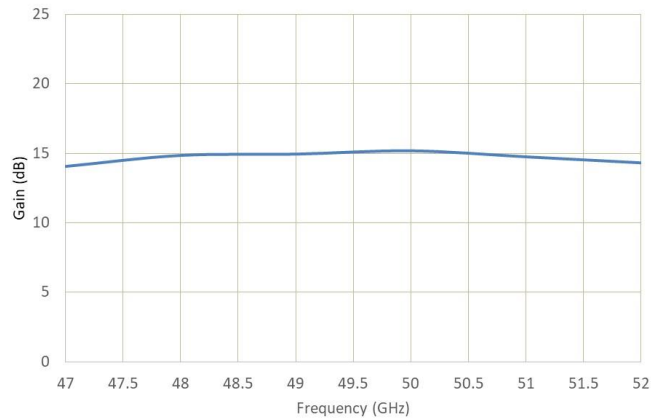
Output Power vs. Frequency (at 21 dBm Input Power)



PAE vs. Frequency (at 21 dBm Input Power)



Gain vs. Frequency (at 21 dBm Input Power)

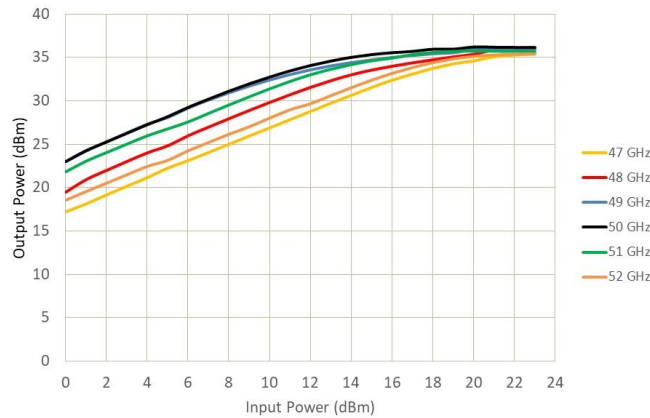


### Large Signal Performance

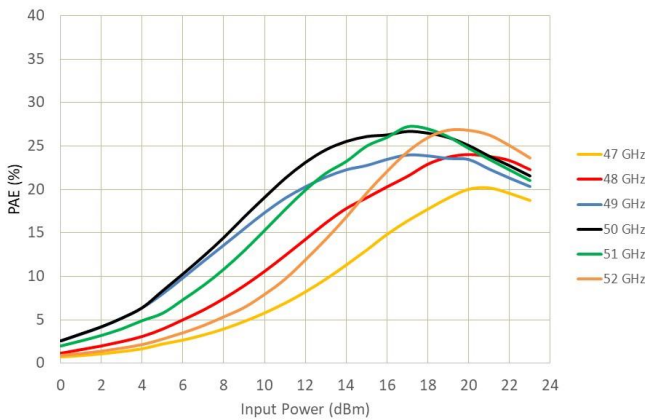
Test Condition:  $V_d = 24\text{ V}$ ,  $I_{dq} = 0.6\text{ A}$

(on-wafer pulsed measurement, typical performance at 25°C)

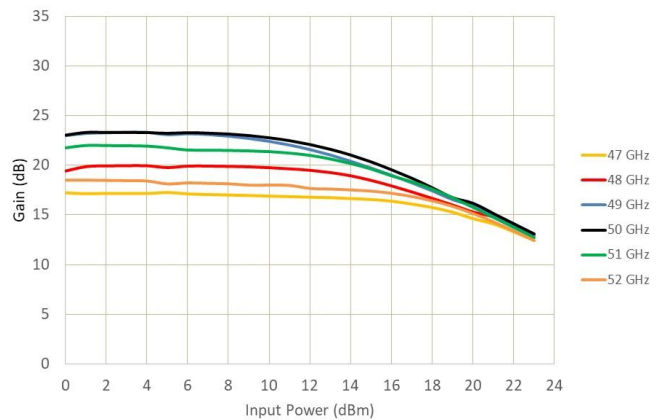
Output Power vs. Input Power vs. Frequency



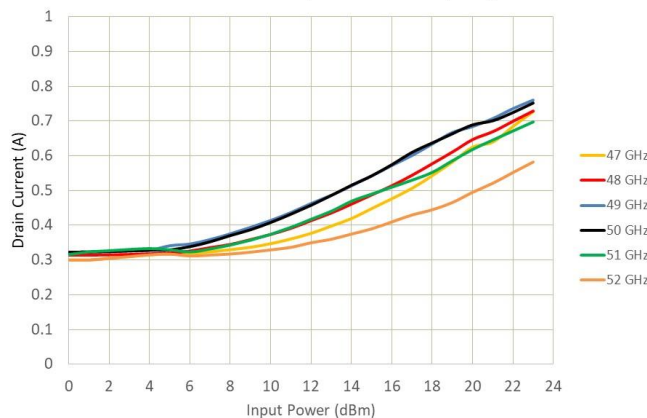
PAE vs. Input Power vs. Frequency



Gain vs. Input Power vs. Frequency



Drain Current vs. Input Power vs. Frequency



### Die Size and Bond Pad Information

Chip Size = 2850 ±25 μm x 1450 ±25 μm

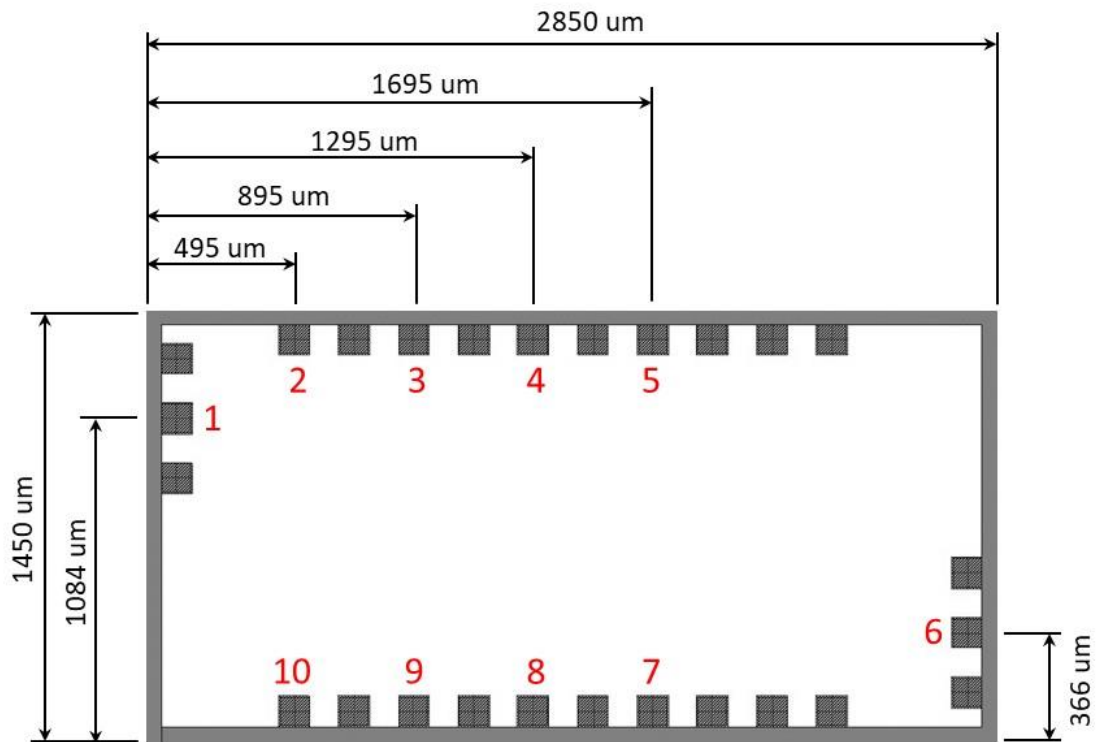
Chip Thickness = 75 μm

Chip Backside metal is ground

RF Input/Output Pad Dimensions = 100 μm x 100 μm

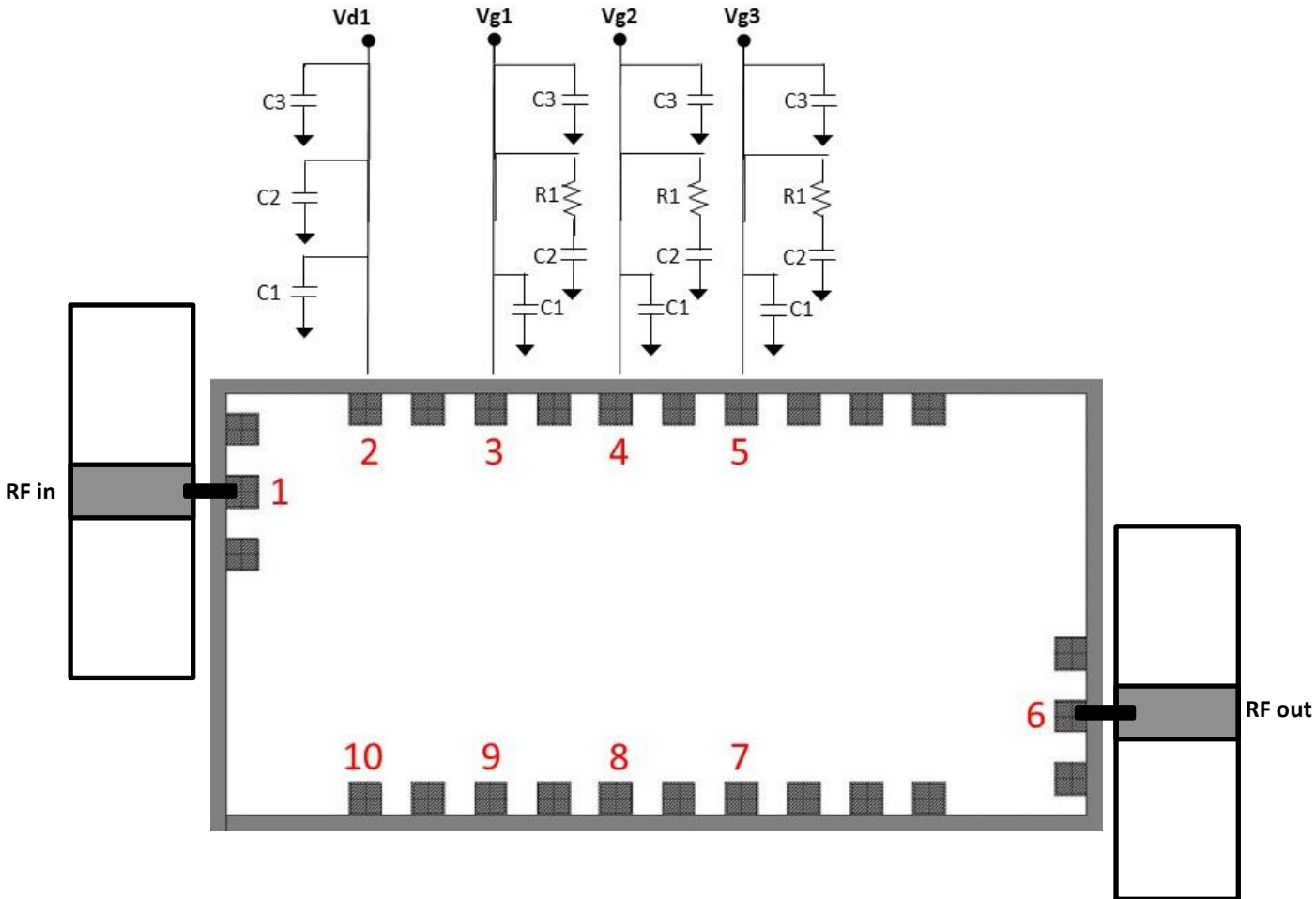
DC Pad Dimensions = 100 μm x 100 μm

Pad Num.	Function
1	RF in
2, 10	Vd1
3, 9	Vg1
4, 8	Vg2
5, 7	Vg3
6	RF out



### Suggested Off-Chip Components

The following diagram shows the recommended off-chip components. Bias can be applied from either top or bottom. Bias does not need to be applied to both sides. All gate connections can be tied together to one source if desired.



### Off-Chip Component Values

Capacitor	Value
C1	100 pF
C2	0.01 $\mu$ F
C3	10 $\mu$ F

Resistor	Value
R1	10 $\Omega$

### Assembly Process

- This product has gold backside metallization and can be mounted using either a high thermal conductive epoxy or AuSn eutectic die attachment.
- Nxbeam recommends the use of AuSn eutectic die attachment due to the high-power level of this product
- Maximum recommended temperature during die attachment is 320 °C for not more than 30 seconds.
- This product contains metal air bridges so caution should be taken when handling the die to avoid damage.

### Bias Information

#### Bias-up Procedure:

- 1.) It is recommended that voltage and current limits are set on the voltage supply's prior to biasing the product.
- 2.) Ensure power supplies are properly grounded to the product test fixture.
- 3.) Apply a negative gate voltage of -6V to Vg1, Vg2, and Vg3 to ensure all devices are pinched off.
- 4.) Gradually increase the drain bias voltage Vd1 to the desired bias level but not to exceed the maximum voltage of 28 V.
- 5.) Gradually increase the gate voltages (Vg1, Vg2, Vg3) independently while monitoring the drain current until the desired drain current in each stage is achieved. Note that the drain connection Vd1 is common to all stages, so each stage current is cumulative on Vd1.
- 6.) Apply RF signal.

#### Bias-down Procedure:

- 1.) Turn off RF signal.
- 2.) Gradually decrease Vg1, Vg2, and Vg3 down to -6 V.
- 3.) Gradually decrease the drain voltage Vd1 down to 0 V.
- 4.) Gradually increase gate voltages (Vg1, Vg2, Vg3) to 0 V.
- 5.) Turn off supply voltages

#### ESD Sensitive Product



### Important Information

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