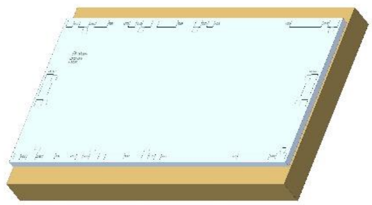
NPA2030-TB-501

27.5 – 31 GHz GaN 19 W Power Amplifier

Product Description

The Nxbeam NPA2030-TB-501 is a Ka-band high power amplifier MMIC fabricated in 0.2um GaN HEMT on SiC mounted on a high thermal conductive heat spreader (tab). The part operates from 27.5 to 31 GHz and provides and average or 19 W of saturated output power, 34% PAE, and 25 dB linear gain at 24V operation. The RF input and output are matched to 50 Ω with DC blocking capacitors for easy system integration. The HEMT devices are fully passivated for reliable operation. Bond pad and heat spreader metallization are Au-based.



Applications

- Ka-band Satellite Communications
- 5G Infrastructure
- Point-to-Point/Multipoint Digital Radios

Key Features (at 24V operation)

- Frequency: 27.5 – 31 GHz
- Linear Gain (Ave.): 25 dB
- Psat (Ave.): 19 W
- PAE (Ave.): 34%

Electrical Specifications

Test Condition: Vd = 24 V, Idq = 1.0 A, CW Performance in Fixture, Typical Performance at 25°C

Parameter		Min	Typical	Max	Unit
Frequency		27		31	GHz
Gain (Small Signal)	27.5 GHz		26		dB
	29 GHz		25.9		
	31 GHz		24.1		
Output Power (at Psat, Pin=22 dBm)	27.5 GHz		43.1		dBm
	29 GHz		43		
	31 GHz		42		
PAE (at Psat, Pin=22 dBm)	27.5 GHz		36.9		%
	29 GHz		34.7		
	31 GHz		31.3		
Power Gain (at Psat, Pin=22 dBm)	27.5 GHz		21.4		dB
	29 GHz		21.4		
	31 GHz		19		
Input Return Loss	27.5 GHz		11		dB
	29 GHz		8		
	31 GHz		25		
Output Return Loss	27.5 GHz		9		dB
	29 GHz		17		
	31 GHz		10		

Absolute Maximum Ratings (Temp. = 25°C)

Parameter	Min	Max	Unit
Drain Voltage (Vd1, Vd2, Vd3)		28	V
Drain Current (Id1)		300	mA
Drain Current (Id2)		720	mA
Drain Current (Id3)		2880	mA
Gate Voltage (Vg1, Vg2, Vg3)	-8	0	V
Input Power (Pin)		TBD	dBm

Recommended Operating Condition

Parameter	Value	Unit
Drain Voltage (Vd)	20 - 28	V
Drain Current (Idq)	up to 1.5	A
Gate Voltage (Vg) (Typical)	-4.1	V

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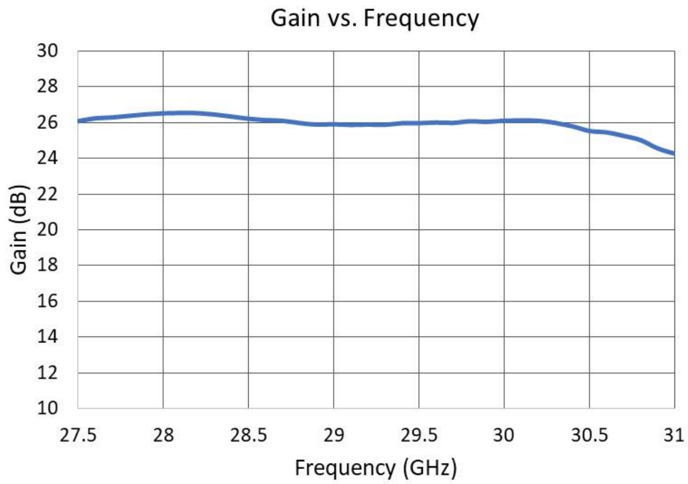
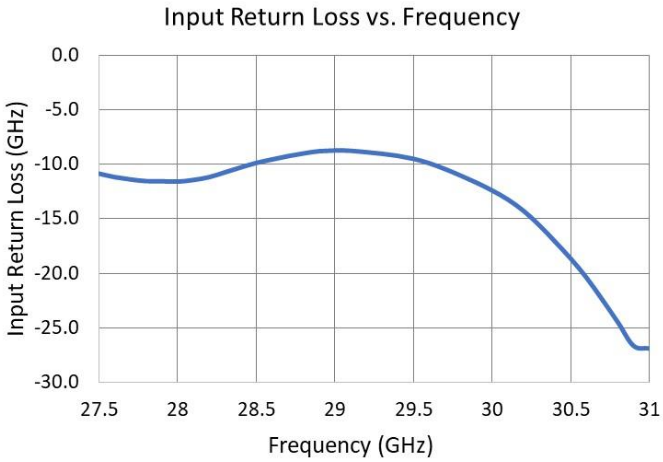
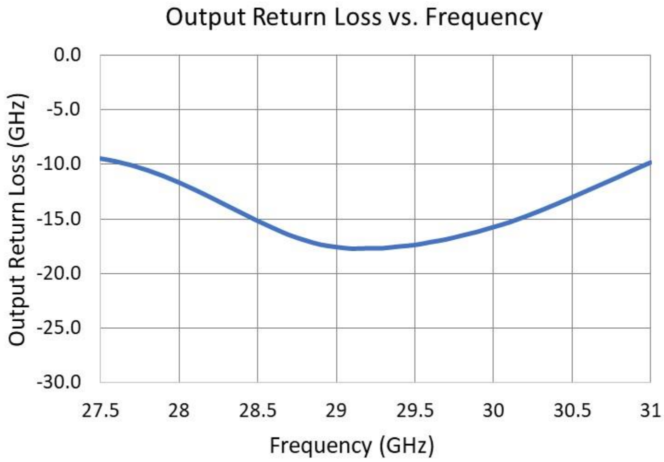
Small Signal Performance

Test Condition: Vd = 24 V, Idq = 1.0 A, (CW Performance in Fixture, Typical Performance at 25°C)







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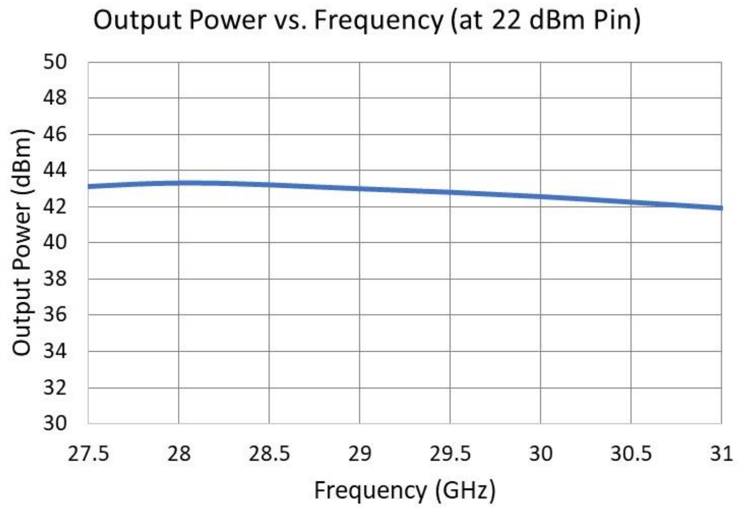
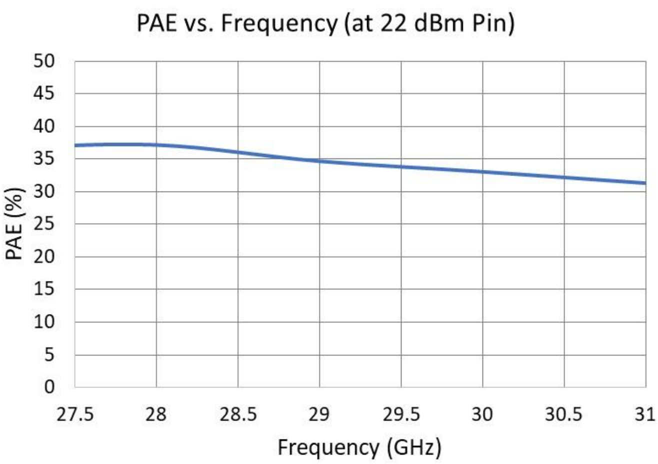
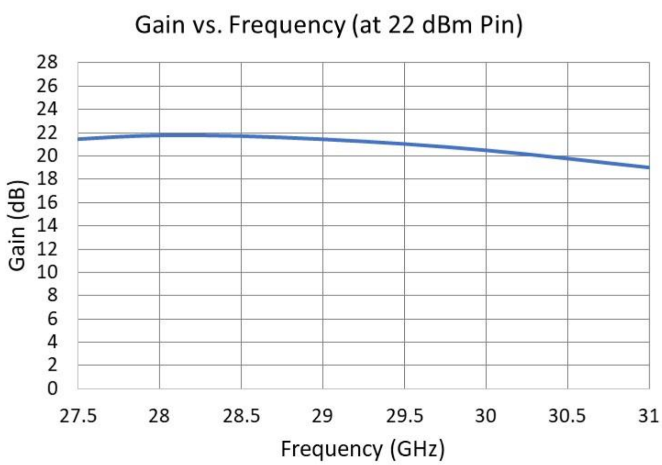
Large Signal Performance

Test Condition: Vd = 24 V, Idq = 1.0 A, Pin = 22 dBm (Psat)
(CW Performance in Fixture, Typical Performance at 25°C)







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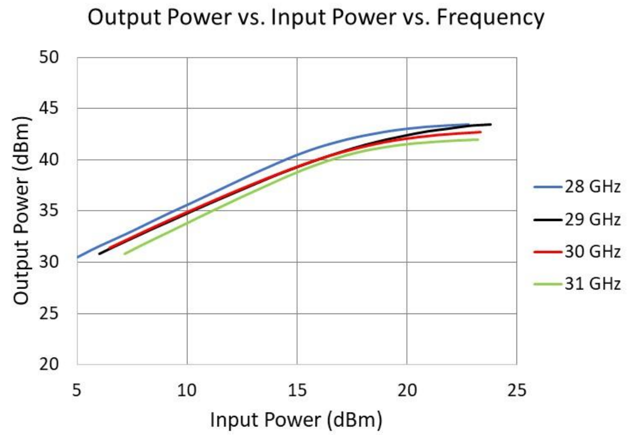
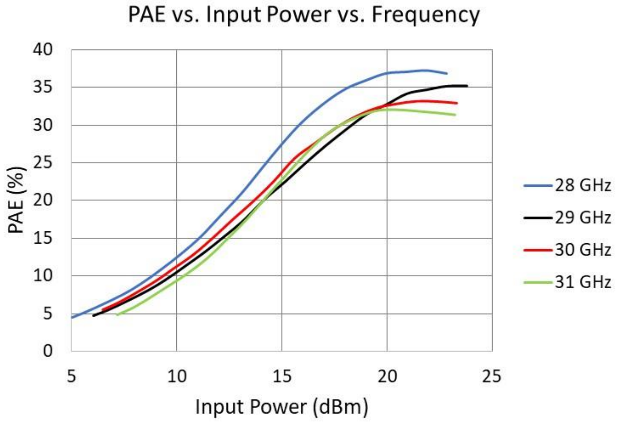
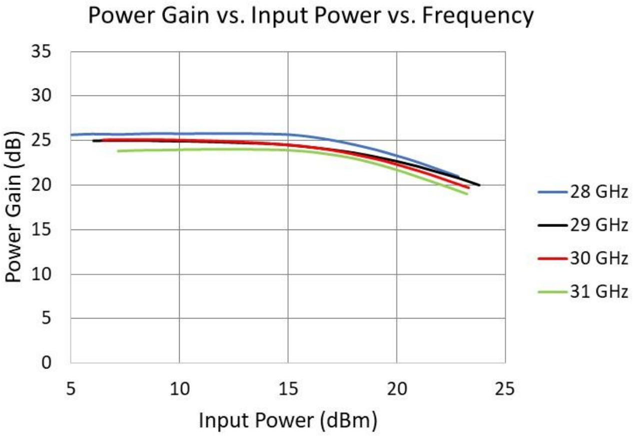
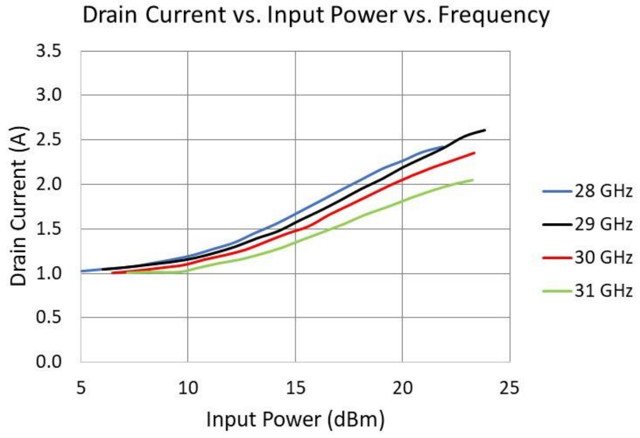
Large Signal Performance

Test Condition: Vd = 24 V, Idq = 1.0 A
(CW Performance in Fixture, Typical Performance at 25°C)









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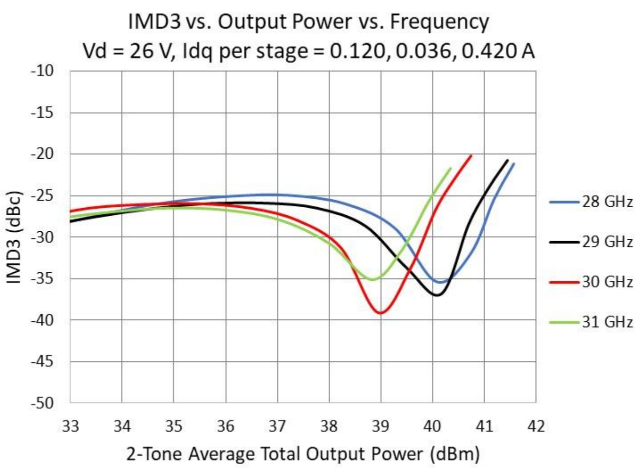
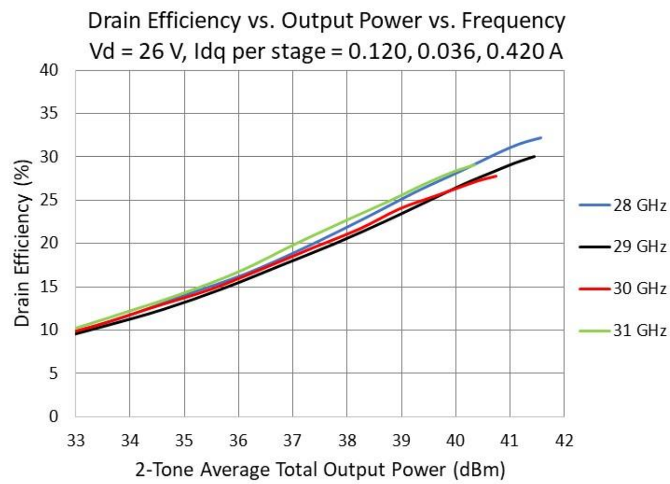
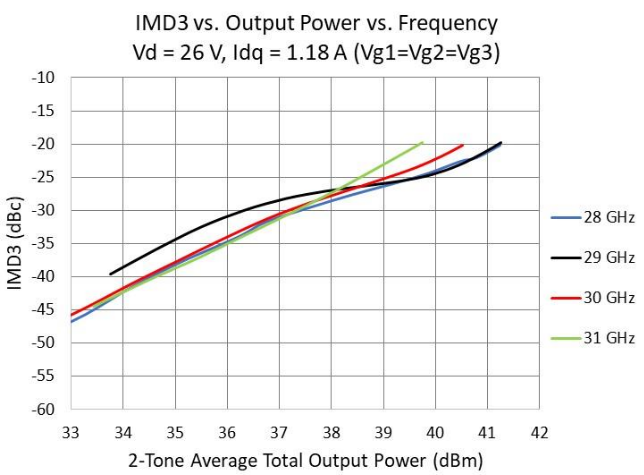
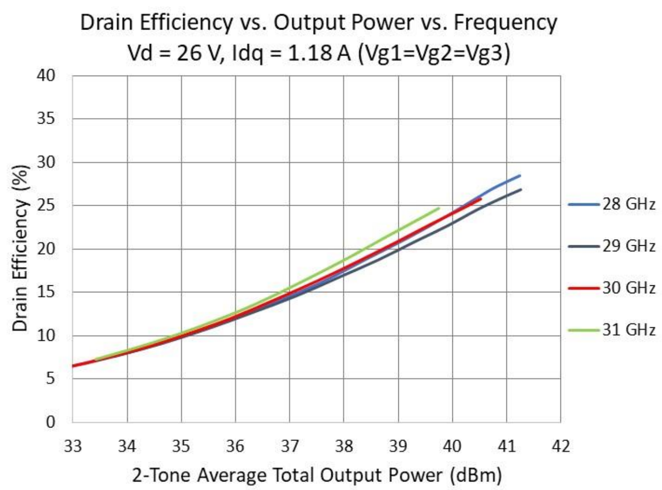
2-Tone Linearity Performance

10 MHz Tone Spacing , CW Performance in Fixture, Typical Performance at 25°C,









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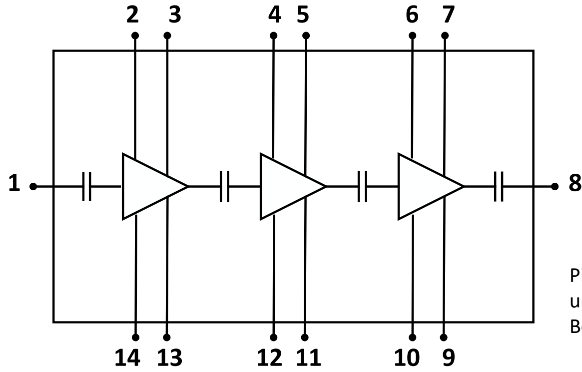
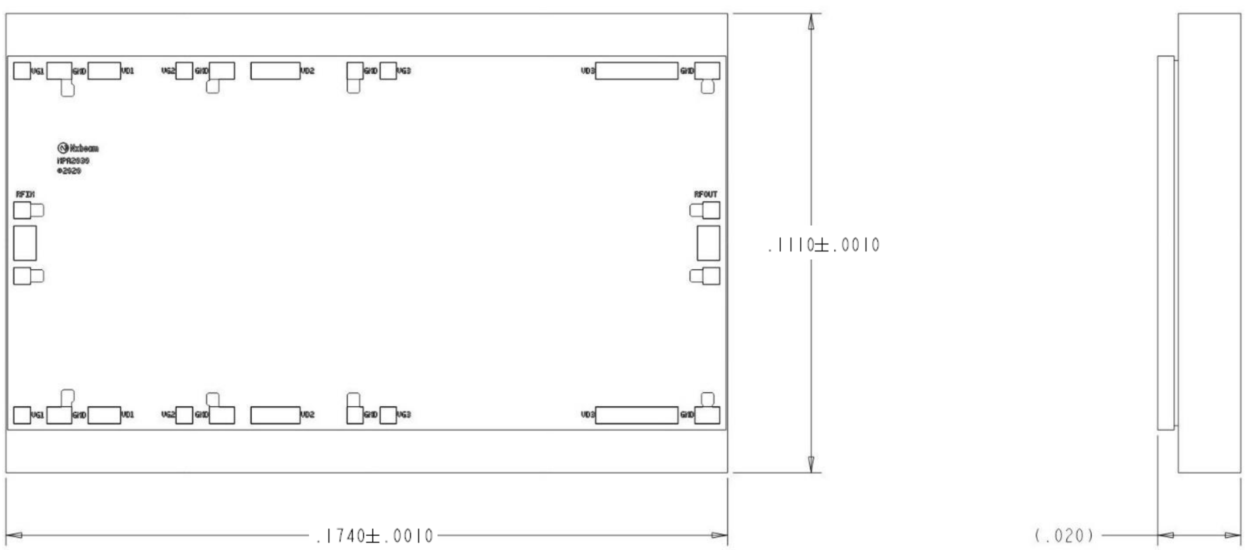
Circuit Block Diagram



Pin number information detailed under Product Dimensions and Bond Pad Information

Product Dimensions
(all dimensions in inches)



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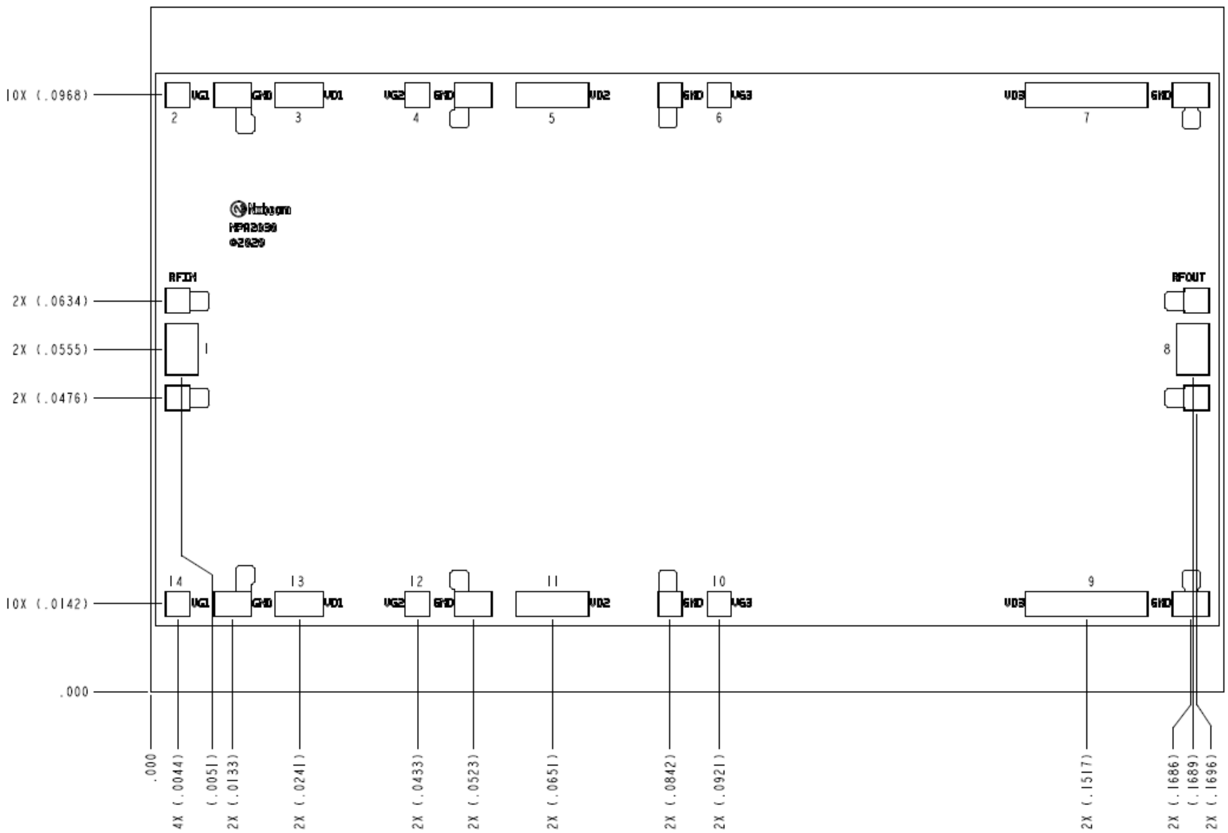
Product Dimensions and Bond Pad Information
(all dimensions in inches unless otherwise noted)

INTERFACE IDENTIFICATION			
ID	FUNCTION	PAD NUMBER	PAD SIZE (MICRONS)
RFIN	RF INPUT	1	134 X 208
RFOUT	RF OUTPUT	8	134 X 208
VG1	GATE VOLTAGE - STAGE 1 (-8V MIN)	2,14	100 X 100
VD1	DRAIN VOLTAGE - STAGE 1 (28V MAX)	3,13	200 X 100
VG2	GATE VOLTAGE - STAGE 2 (-8V MIN)	4,12	100 X 100
VD2	DRAIN VOLTAGE - STAGE 2 (28V MAX)	5,11	300 X 100
VG3	GATE VOLTAGE - STAGE 3 (-8V MIN)	6,10	100 X 100
VD3	DRAIN VOLTAGE - STAGE 3 (28V MAX)	7,9	500 X 100



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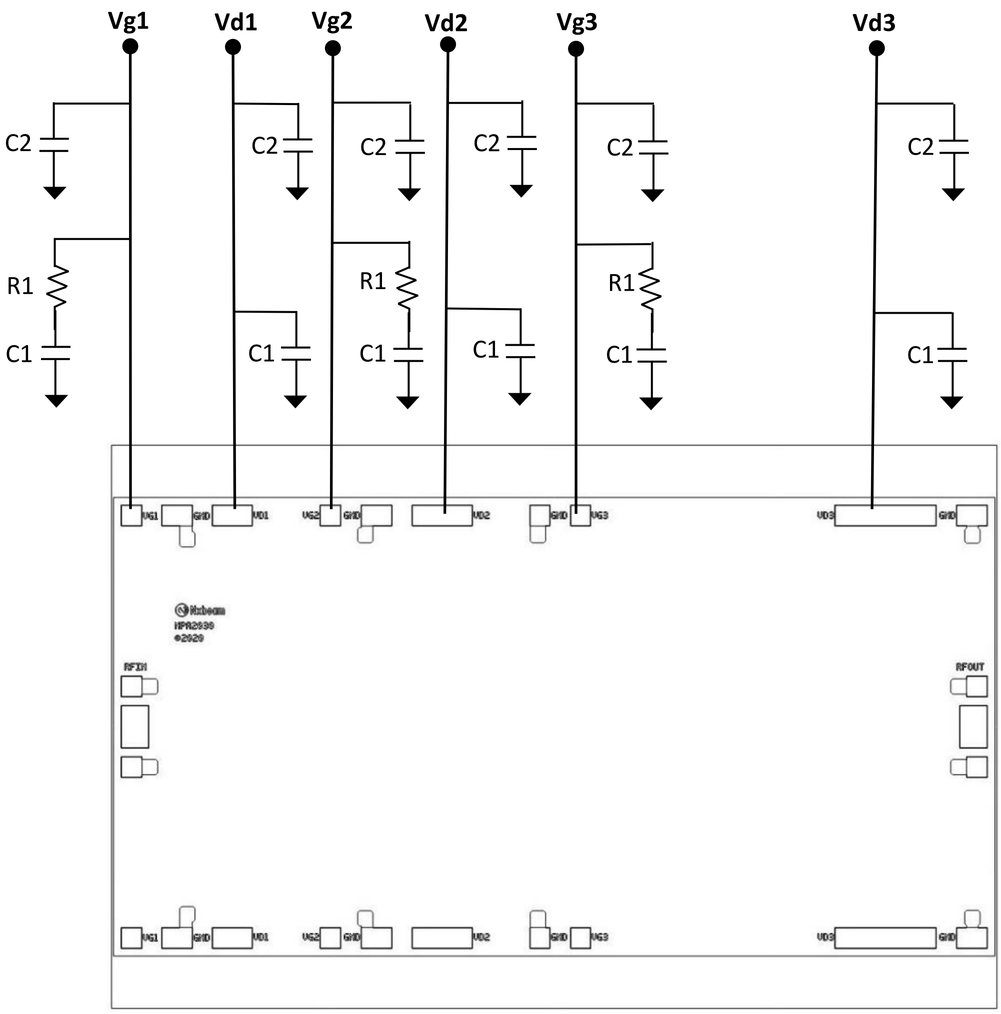
Suggested Off-Chip Components

The following diagram is a suggested bonding arraignment with off-chip components. All drain connections can be tied together to one source. All gate connections can be tied together to one source if desired. The NPA2030-TB-501 can be biased from either top or bottom of the chip as well as from both sides if desired.



Off-Chip Component Values

Capacitor	Value
C1	0.01 µF
C2	1 µF

Resistor	Value
R1	10 Ω

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Assembly Process

- The heat spreader is gold plated and can be mounted using either a high thermal conductive epoxy or solder attachment.
- Maximum recommended temperature during product attachment is 260 °C for not more than 30 seconds.
- This product contains metal air bridges so caution should be taken when handling to avoid damage.

Bias Information

The NPA2030-TB-501 can be biased from either top or bottom of the chip as well as from both sides if desired.

Bias-up Procedure:

1.) It is recommended that voltage and current limits are set on the voltage supply's prior to biasing the product.
2.) Ensure power supplies are properly grounded to the product test fixture.
3.) Apply a negative gate voltage of -6V to Vg1, Vg2, and Vg3 to ensure all devices are pinched off.
4.) Gradually increase the drain bias voltage (Vd1, Vd2, Vd3) to the desired bias level but not to exceed the maximum voltage of 28 V.
5.) Gradually increase the gate voltages (Vg1, Vg2, Vg3) while monitoring the drain current until the desired drain current in each stage is achieved.
6.) Apply RF signal.

Bias-down Procedure:

1.) Turn off RF signal.
2.) Gradually decrease Vg1, Vg2, and Vg3 down to -6 V.
3.) Gradually decrease the drain voltages (Vd1, Vd2, Vd3) down to 0 V.
4.) Gradually increase gate voltages (Vg1, Vg2, Vg3) to 0 V.
5.) Turn off supply voltages

ESD Sensitive Product

Important Information

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The product represented by this datasheet is subject to U.S. Export Law as contained in ITAR or the EAR regulations.

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