

Product Description

The Nxbeam NPA7000-DE is a E-band power amplifier MMIC fabricated in 0.09um GaN HEMT on SiC. This part is ideally suited for E-band satellite and point-to-point communications applications. The MMIC operates from 65 to 76 GHz and provides 1 W saturated output power, 27% PAE, and 13 dB of linear gain. The NPA7000-DE comes in die form with RF input and output matched to 50 Ω with DC blocking capacitors for easy system integration. The HEMT devices are fully passivated for reliable operation. Bond pad and backside metallization are Au-based for compatibility with eutectic die attachment methods.



Applications

- E-band Satellite Communications
- 5G Infrastructure
- Point-to-Point/Multipoint Digital Radios

Key Features

- Frequency: 65 – 76 GHz
- Linear Gain (Ave.): 13 dB
- Psat (Ave.): 1 W
- PAE (Ave.): 27%
- Chip Dimensions: 1.575 x 0.875 x 0.050 mm

Electrical Specifications

Test Condition: Vd = 15 V, Idq = 120 mA, CW Measurements

Parameter		Min	Typical	Max	Unit
Frequency		65		76	GHz
Gain (Small Signal)	65 GHz		12.3		dB
	71 GHz		13.7		
	76 GHz		9.5		
Output Power (at Psat, Pin=21 dBm)	65 GHz		30.5*		dBm
	71 GHz		30.1		
	75 GHz		30.0		
PAE (at Psat, Pin=21 dBm)	65 GHz		32*		%
	71 GHz		29		
	75 GHz		28		
Power Gain (at Psat, Pin=21 dBm)	65 GHz		9*		dB
	71 GHz		9.5		
	75 GHz		8.8		
Input Return Loss	65 GHz		7		dB
	71 GHz		13		
	76 GHz		5		
Output Return Loss	65 GHz		9		dB
	71 GHz		6		
	76 GHz		7		

* Power measurements were conducted from 71 to 75 GHz due to test set limitations. Lower frequency power data is estimated based on simulation data.

Absolute Maximum Ratings (Temp. = 25°C)

Parameter	Min	Max	Unit
Drain Voltage (Vd1)		20	V
Drain Current (Id1) from Stage 1		100	mA
Drain Current (Id1) from Stage 2		200	mA
Gate Voltage (Vg1, Vg2, Vg3)	-8	0	V

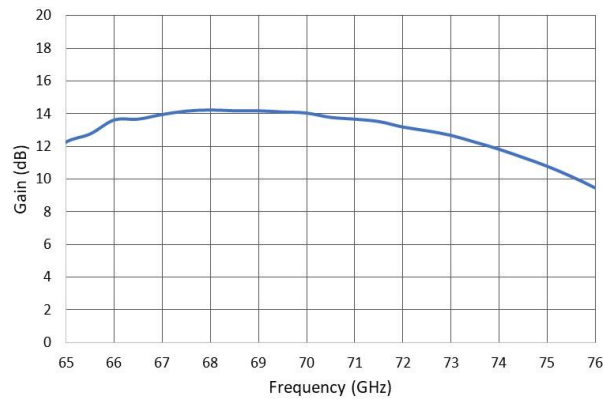
Recommended Operating Condition

Parameter	Value	Unit
Drain Voltage (Vd)	10 to 20	V
Drain Current (Id1) from Stage 1	up to 40	mA
Drain Current (Id1) from Stage 2	up to 80	mA
Gate Voltage (Vg1, Vg2) (Typical)	-4.1	V

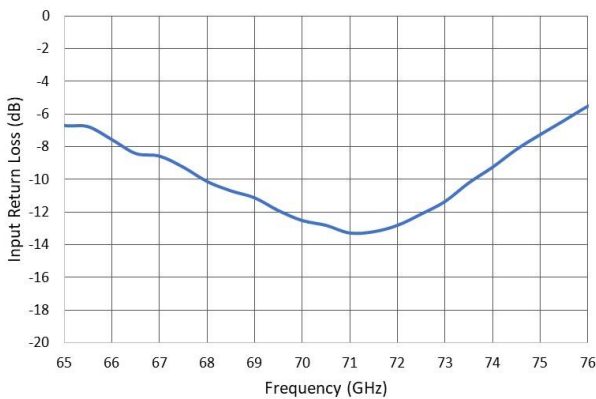
Small Signal Performance

Test Condition: Vd = 15 V, Idq = 120 mA, CW measurement

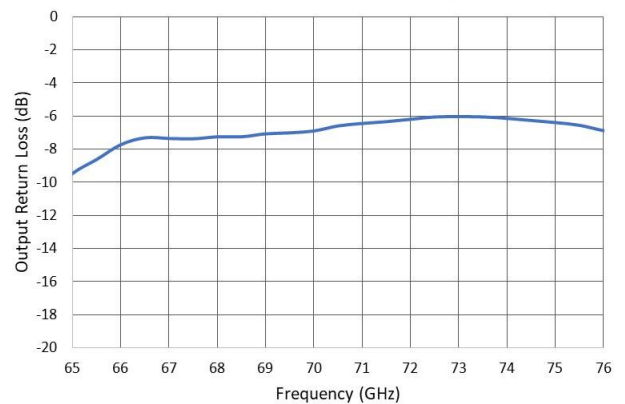
Gain vs. Frequency



Input Return Loss vs. Frequency



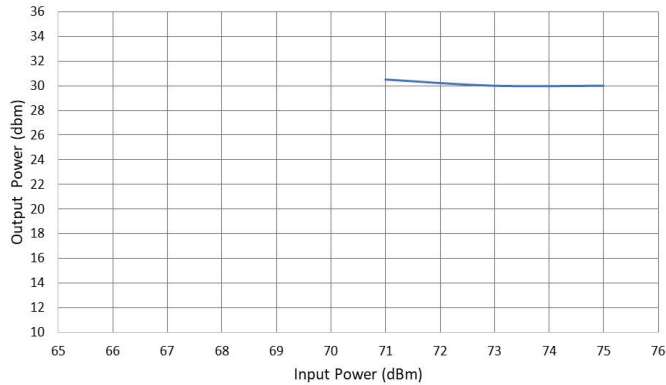
Output Return Loss vs. Frequency



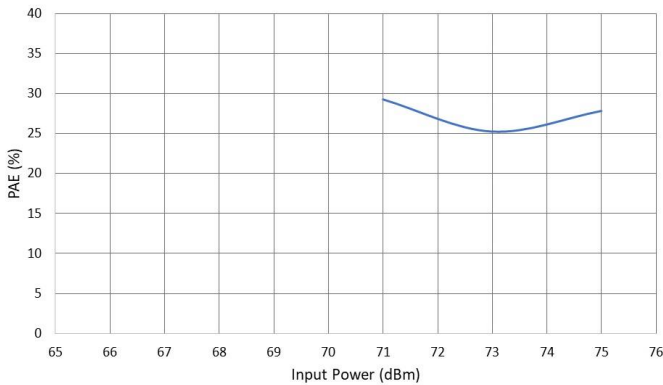
Large Signal Performance

Test Condition: $V_d = 15\text{ V}$, $I_{dq} = 120\text{ mA}$, CW measurement
(Power Measurement Capability only from 71 to 75 GHz)

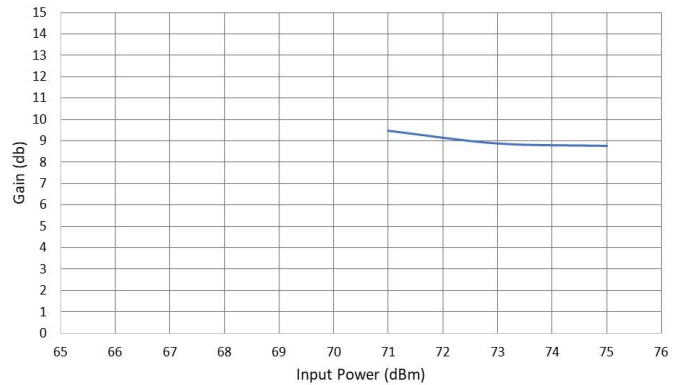
Output Power vs. Frequency (at 21 dBm Input Power)



PAE vs. Frequency (at 21 dBm Input Power)



Gain vs. Frequency (at 21 dBm Input Power)

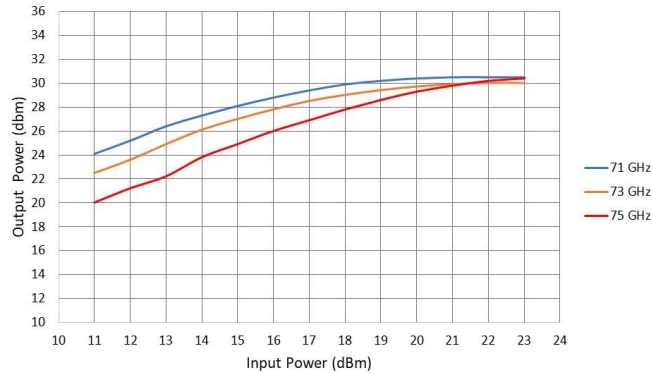


Large Signal Performance

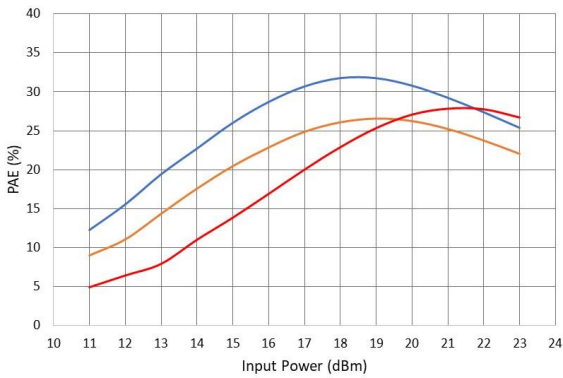
Test Condition: $V_d = 15\text{ V}$, $I_{dq} = 120\text{ mA}$, CW measurement

(Power Measurement Capability only from 71 to 75 GHz)

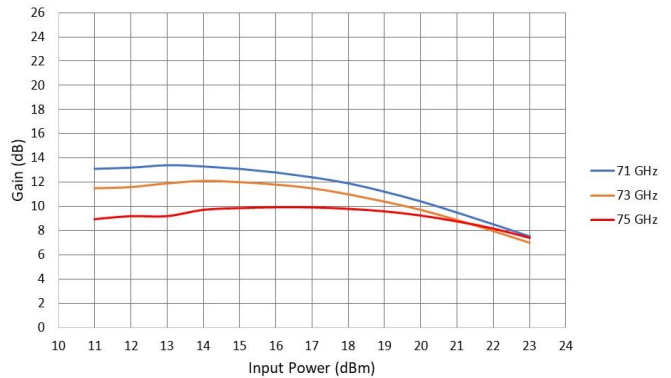
Output Power vs. Input Power vs. Frequency



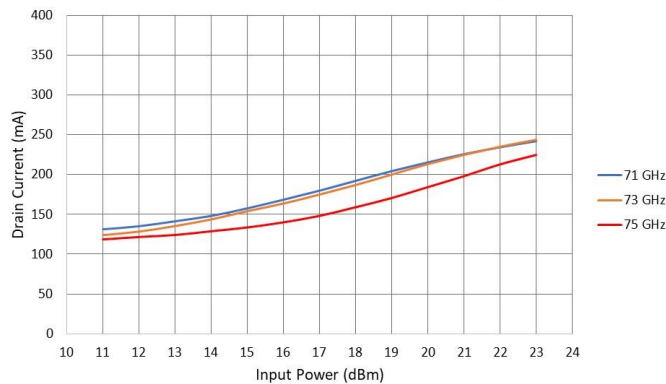
PAE vs. Input Power vs. Frequency



Gain vs. Input Power vs. Frequency



Drain Current vs. Input Power vs. Frequency



Die Size and Bond Pad Information

Chip Size = $1575 \pm 25 \mu\text{m} \times 875 \pm 25 \mu\text{m}$

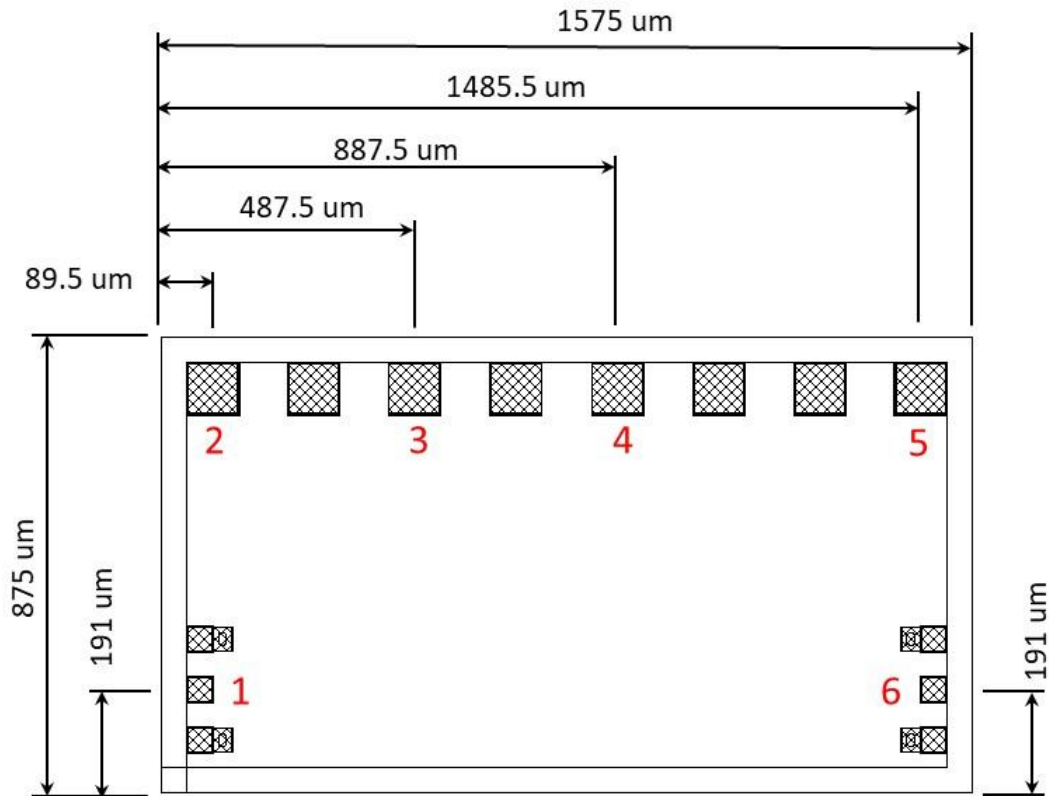
Chip Thickness = $50 \mu\text{m}$

Chip Backside metal is ground

RF Input/Output Pad Dimensions = $50 \mu\text{m} \times 50 \mu\text{m}$

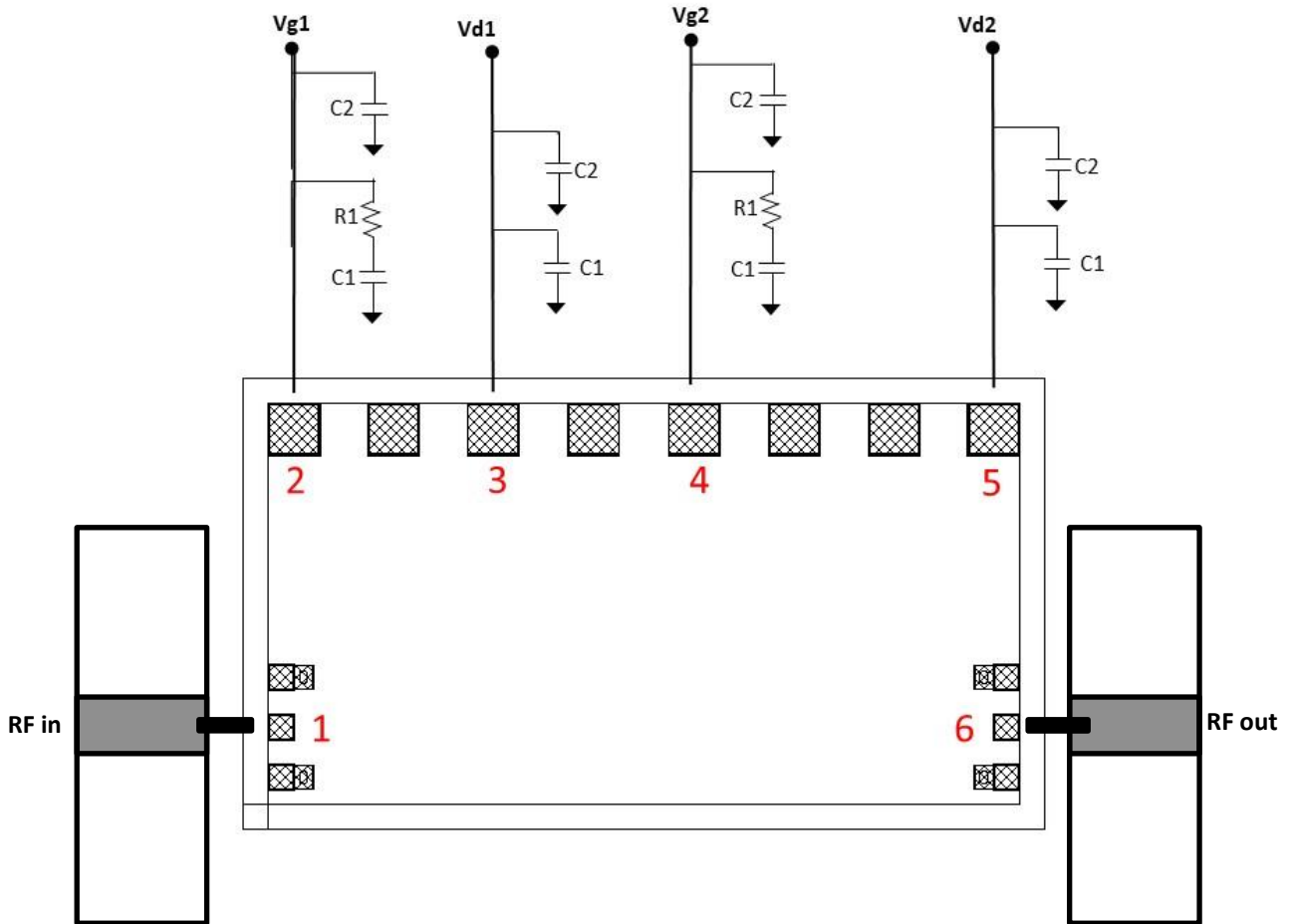
DC Pad Dimensions = $100 \mu\text{m} \times 100 \mu\text{m}$

Pad Num.	Function
1	RF in
2	Vg1
3	Vd1
4	Vg2
5	Vd3
6	RF out



Suggested Off-Chip Components

The following diagram shows the recommended off-chip components. All gate connections can be tied together to one source if desired.



Off-Chip Component Values

Capacitor	Value
C1	0.01 μ F
C2	10 μ F

Resistor	Value
R1	10 Ω

Assembly Process

- This product has gold backside metallization and can be mounted using either a high thermal conductive epoxy or AuSn eutectic die attachment.
- Maximum recommended temperature during die attachment is 320 °C for not more than 45 seconds.
- This product contains metal air bridges so caution should be taken when handling the die to avoid damage.

Bias Information

Bias-up Procedure:

- 1.) It is recommended that voltage and current limits are set on the voltage supply's prior to biasing the product.
- 2.) Ensure power supplies are properly grounded to the product test fixture.
- 3.) Apply a negative gate voltage of -7V to Vg1 and Vg2 to ensure all devices are pinched off.
- 4.) Gradually increase the drain bias voltage Vd1 and Vd2 to the desired bias level but not to exceed the maximum voltage of 20 V.
- 5.) Gradually increase the gate voltages Vg1 and Vg2 while monitoring the drain current until the desired drain current in each stage is achieved.
- 6.) Apply RF signal.

Bias-down Procedure:

- 1.) Turn off RF signal.
- 2.) Gradually decrease Vg1 and Vg2 down to -7 V.
- 3.) Gradually decrease the drain voltage Vd1 and Vd2 down to 0 V.
- 4.) Gradually increase gate voltages Vg1 and Vg2 to 0 V.
- 5.) Turn off supply voltages

ESD Sensitive Product



Important Information

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