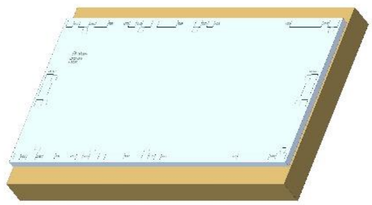
NPA2001-TB-501

26.5 – 29.5 GHz GaN 35 W Power Amplifier

Product Description

The Nxbeam NPA2001-TB-501 is a Ka-band high power amplifier MMIC fabricated in 0.2um GaN HEMT on SiC mounted on a high thermal conductive heat spreader (tab). The MMIC operates from 26.5 to 29.5 GHz and provides 35 W saturated output power, 31% PAE, and 25 dB of linear gain. The NPA2001-TB-501 comes in die-on-tab form with RF input and output matched to 50 Ω with DC blocking capacitors for easy system integration. The HEMT devices are fully passivated for reliable operation. Bond pad and backside metallization are Au-based for compatibility with eutectic die attachment methods.



Applications

- 5G mmWave (n257)
- Ka-band Satellite Communications
- Point-to-Point/Multipoint Digital Radios

Key Features

- Frequency: 26.5 – 29.5 GHz
- Linear Gain: 25 dB
- Psat: 35 W
- PAE: 31%

Electrical Specifications

Test Condition: Vd = 24 V , Idq = 2.18 A, CW Performance in Fixture, Typical Performance at 25°C

Parameter		Min	Typical	Max	Unit
Frequency		26.5		29.5	GHz
Gain (Small Signal)	27 GHz		25		dB
	28 GHz		25		
	29 GHz		25		
Output Power (at Psat, Pin=26 dBm)	27 GHz		45.6		dBm
	28 GHz		45.4		
	29 GHz		45.4		
PAE (at Psat, Pin=26 dBm)	27 GHz		32.5		%
	28 GHz		31.4		
	29 GHz		31.0		
Power Gain (at Psat, Pin=26 dBm)	27 GHz		20.5		dB
	28 GHz		20.3		
	29 GHz		19.7		
Input Return Loss	27 GHz		20		dB
	28 GHz		12		
	29 GHz		15		
Output Return Loss	27 GHz		14		dB
	28 GHz		14		
	29 GHz		13		

Maximum Quiescent Bias

Parameter	Max	Unit
Drain Voltage (Vd1, Vd2, Vd3)	28	V
Drain Current (Id1)	264	mA
Drain Current (Id2)	640	mA
Drain Current (Id3)	2560	mA

Maximum quiescent bias represents the operational bias used during reliability life testing. Biasing the part at or below this bias ensures reliability will be bound by the published reliability results.

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Absolute Maximum Ratings (Temp. = 25°C)

Parameter	Min	Max	Unit
Drain Voltage (Vd1, Vd2, Vd3)		28	V
Drain Current (Id1)		660	mA
Drain Current (Id2)		1600	mA
Drain Current (Id3)		6400	mA
Gate Voltage (Vg1, Vg2, Vg3)	-8	0	V

Absolute maximum ratings represent the maximum current under power saturation conditions.

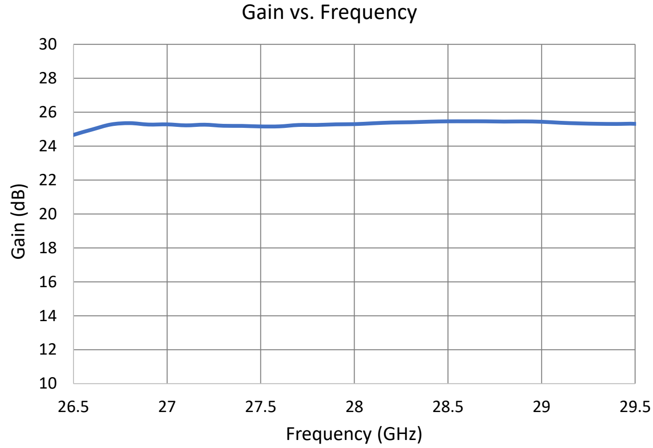
Recommended Quiescent Operating Condition

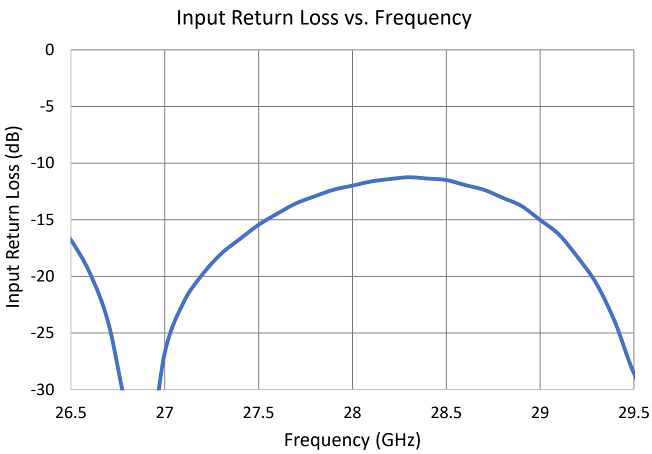
Parameter	Value	Unit
Drain Voltage (Vd)	20 - 28	V
Drain Current (Id1)	up to 264	mA
Drain Current (Id2)	up to 640	mA
Drain Current (Id3)	up to 2560	mA
Gate Voltage (Vg) (Typical Range)	-4	V

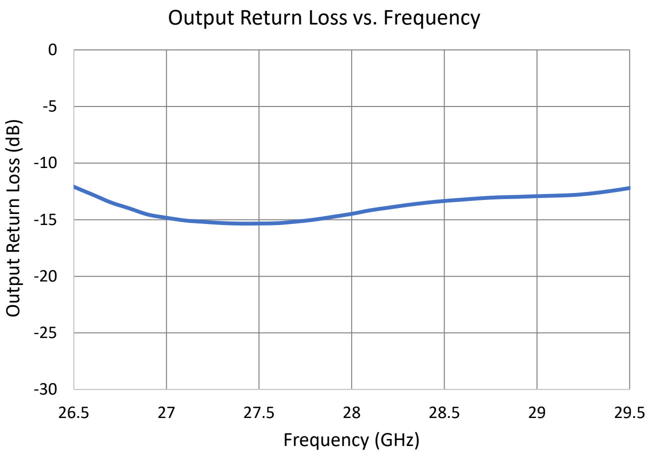
Gate voltage will vary based on desired current per stage

Small Signal Performance

Test Condition: Vd = 24 V, Idq = 2.18 A, (CW Performance in Fixture, Typical Performance at 25°C)







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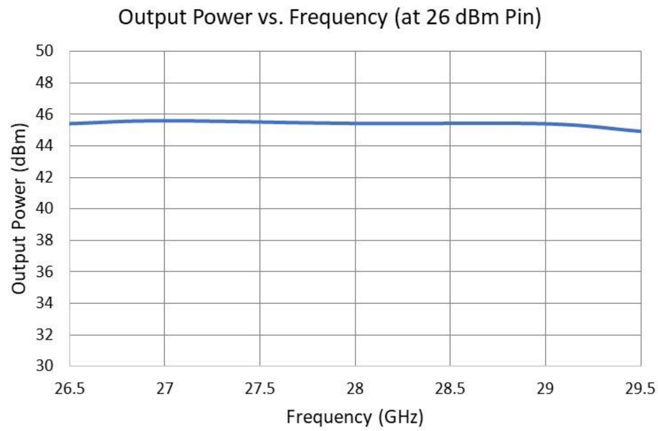
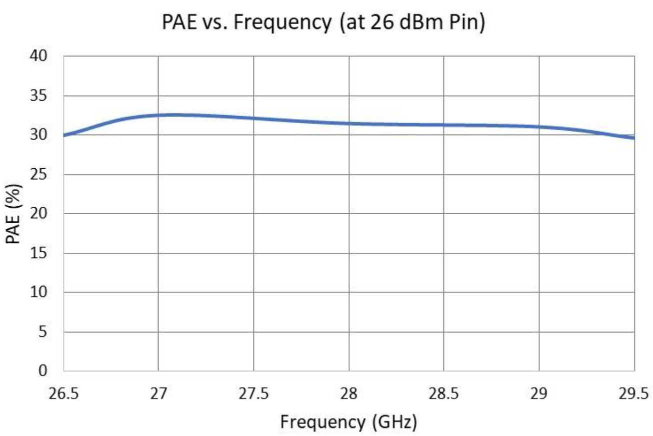
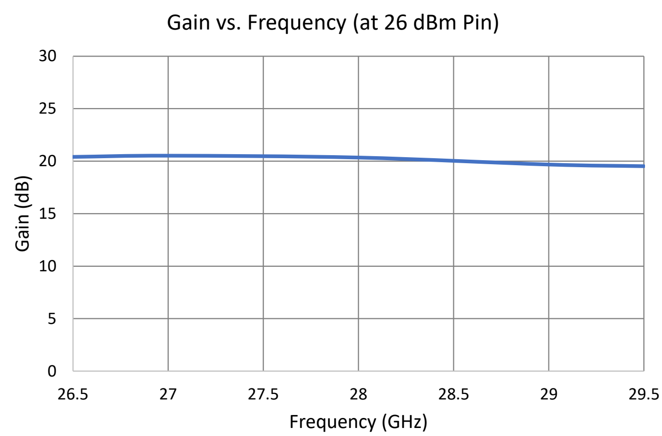
Large Signal Performance

Test Condition: Vd = 24 V, Idq = 2.18 A, Pin = 26 dBm (Psat)
(CW Performance in Fixture, Typical Performance at 25°C)







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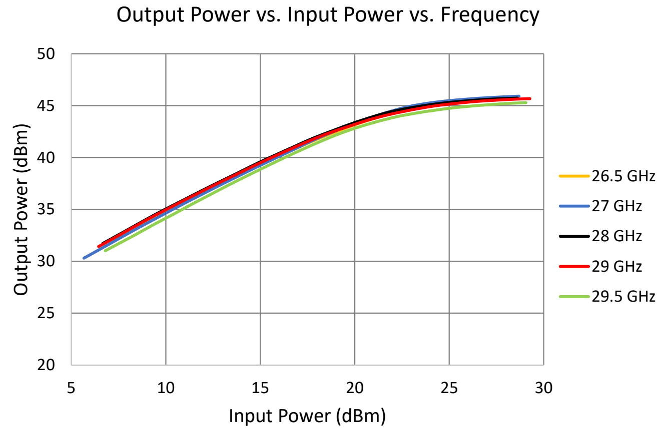
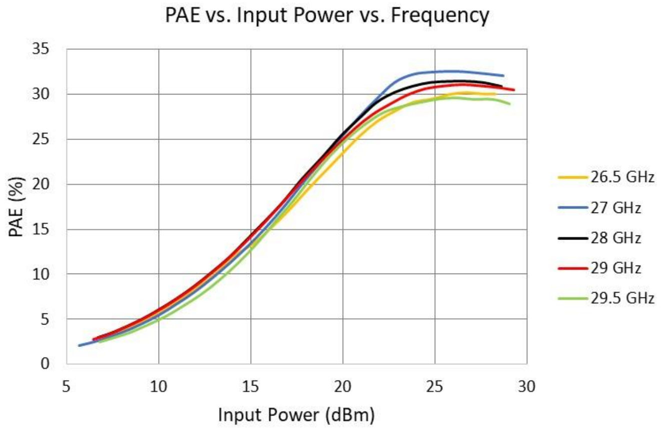
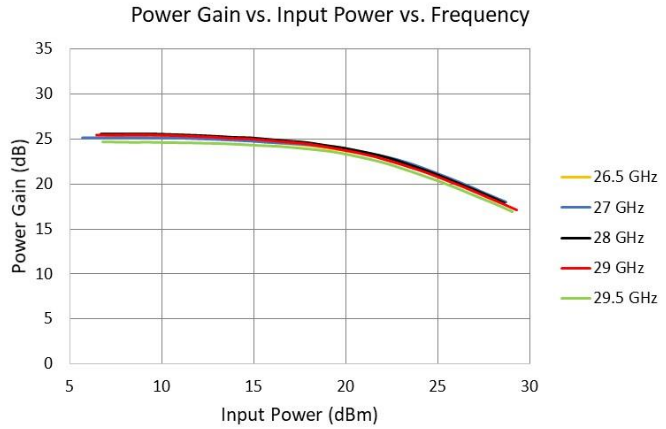
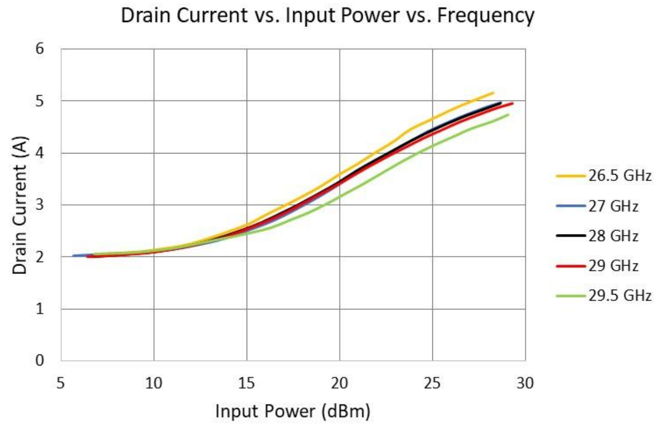
Large Signal Performance

Test Condition: Vd = 24 V, Idq = 2.18 A,
(CW Performance in Fixture, Typical Performance at 25°C)









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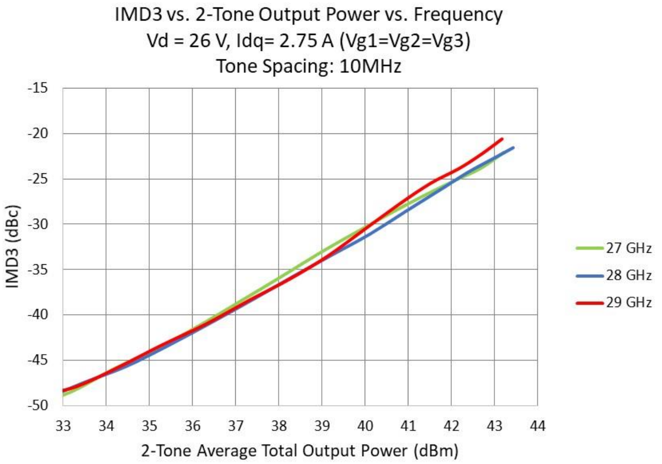
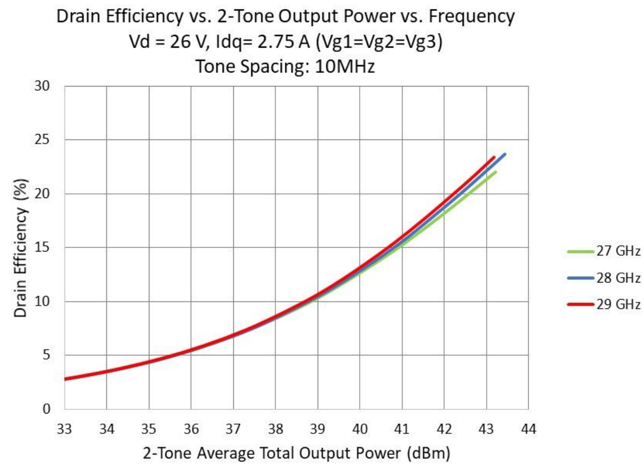
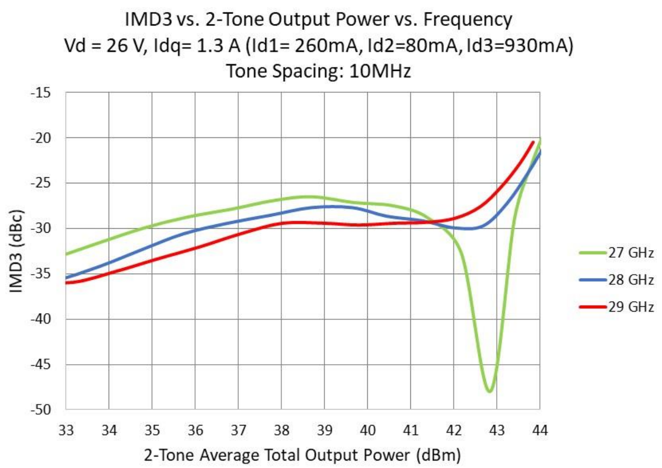
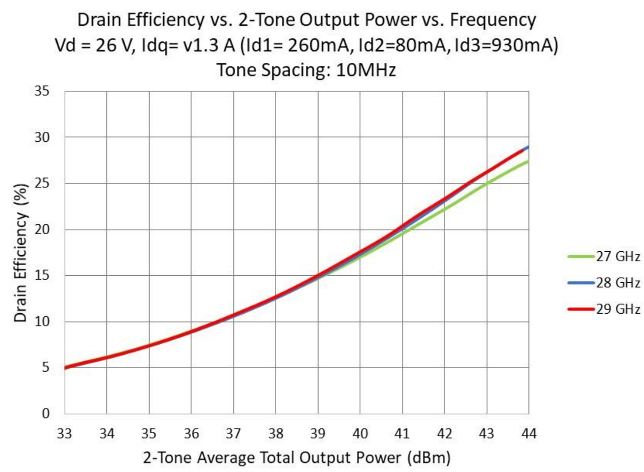
2-Tone Linearity Performance

CW Performance in Fixture, Typical Performance at 25°C,
Bias as Listed in Figure









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Thermal Information

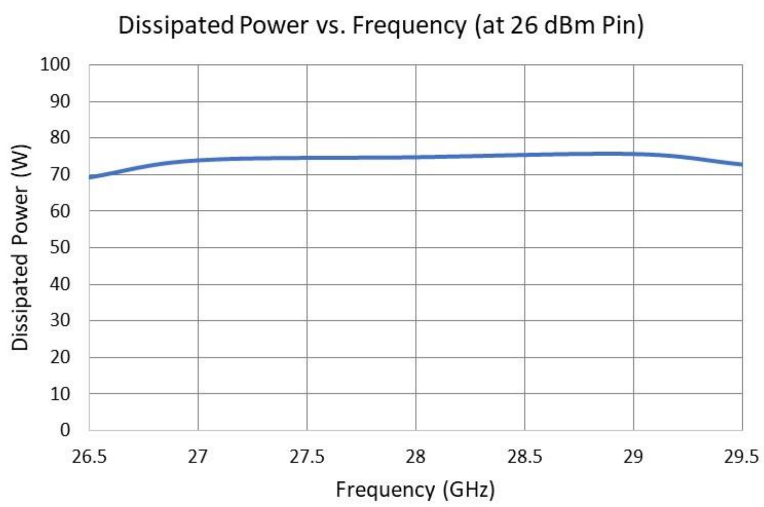
RF = Off

Parameter	Condition	Value	Unit
Thermal Resistance ($R_{\Theta JC}$)	RF=OFF	1.24	°C/W
Junction Temperature (Tj)	$T_{backside}$=85 °C, V_d=24 V, I_{dq}=2.18 A, P_{dis}=52.3 W	149.9	°C

RF = On, Peak Junction Temperature at Pin = 26 dBm (Psat), CW Performance in Fixture

Parameter	Condition	Value	Unit
Thermal Resistance ($R_{\Theta JC}$)	P_{in}=26 dBm, Freq.=29 GHz	1.29	°C/W
Junction Temperature (Tj)	$T_{backside}$=85 °C, V_d=24 V, I_d=4.59 A, P_{dis}=75.7 W	182.7	°C

Note 1: Thermal resistance determined to the back of the tab.
Note 2: Mean time to failure per junction temperature information can be found in the following document: Nxbeam_GaN20MMIC_Reliability.pdf



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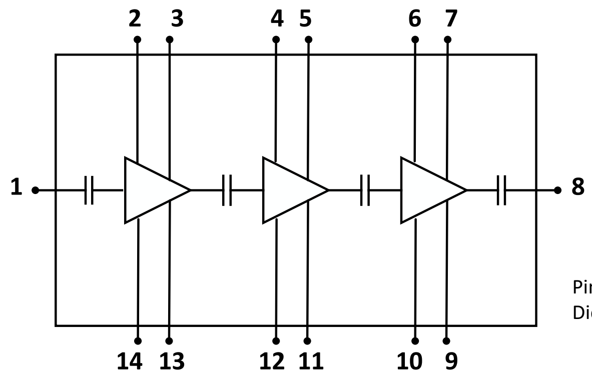
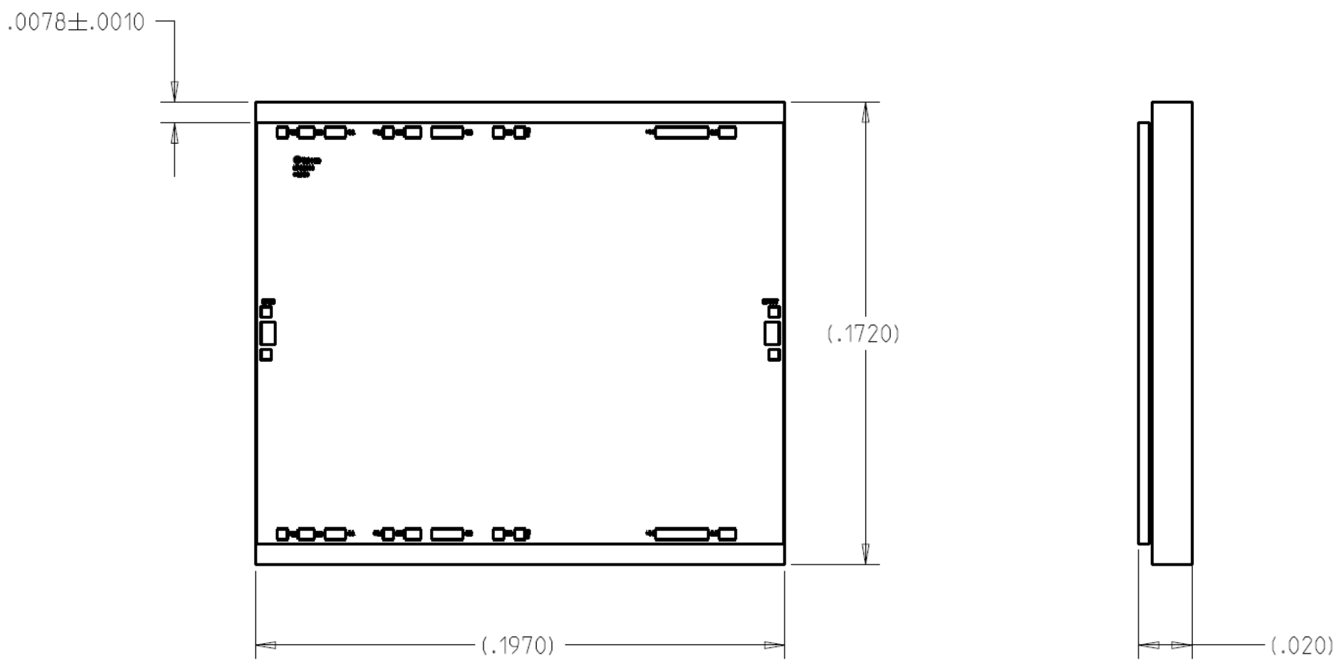
Circuit Block Diagram



Pin number information detailed under Die Size and Bond Pad Information

Product Dimensions
(all dimensions in inches)



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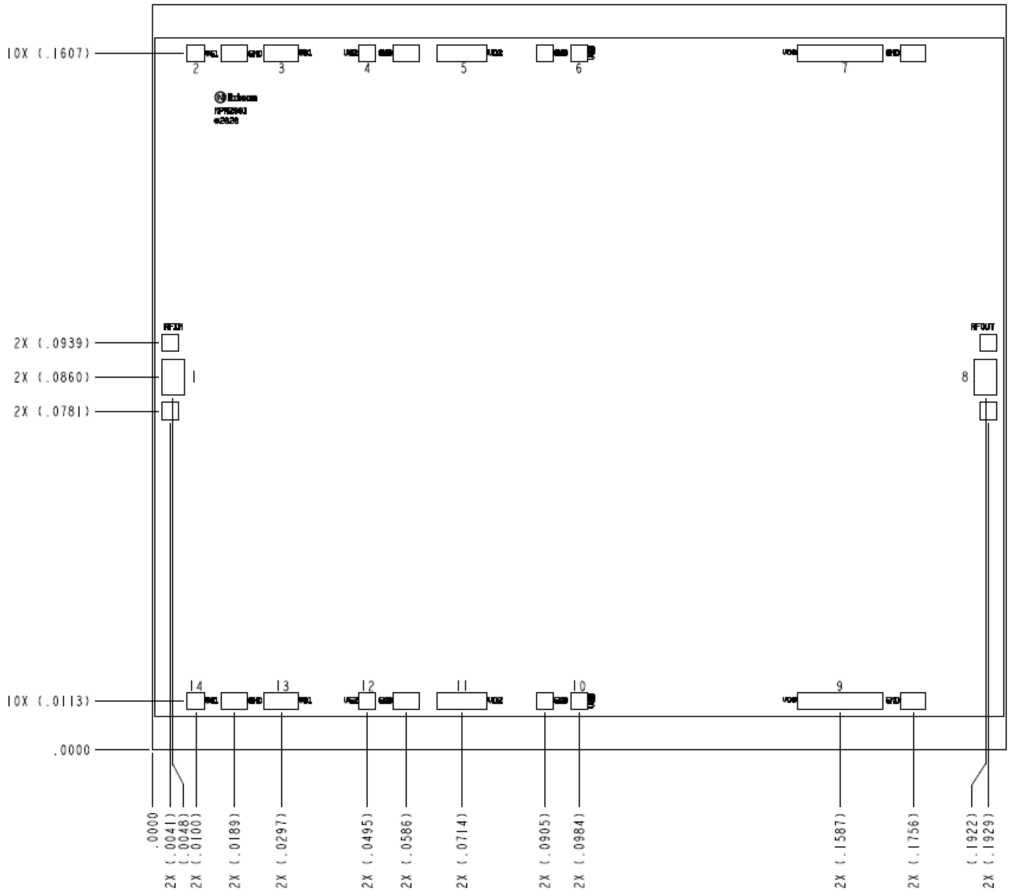
Die Size and Bond Pad Information

TABLE I: INTERFACE IDENTIFICATION			
ID	FUNCTION	PAD NUMBER	PAD SIZE (MICRONS)
RFIN	RF INPUT	1	134 X 208
RFOUT	RF OUTPUT	8	134 X 208
VG1	GATE VOLTAGE - STAGE 1 (-8V MIN, 0V MAX)	2,14	100 X 100
VD1	DRAIN VOLTAGE - STAGE 1 (0V MIN, 28V MAX)	3,13	196 X 100
VG2	GATE VOLTAGE - STAGE 2 (-8V MIN, 0V MAX)	4,12	100 X 100
VD2	DRAIN VOLTAGE - STAGE 2 (0V MIN, 28V MAX)	5,11	296 X 100
VG3	GATE VOLTAGE - STAGE 3 (-8V MIN, 0V MAX)	6,10	96 X 100
VD3	DRAIN VOLTAGE - STAGE 3 (0V MIN, 28V MAX)	7,9	500 X 100



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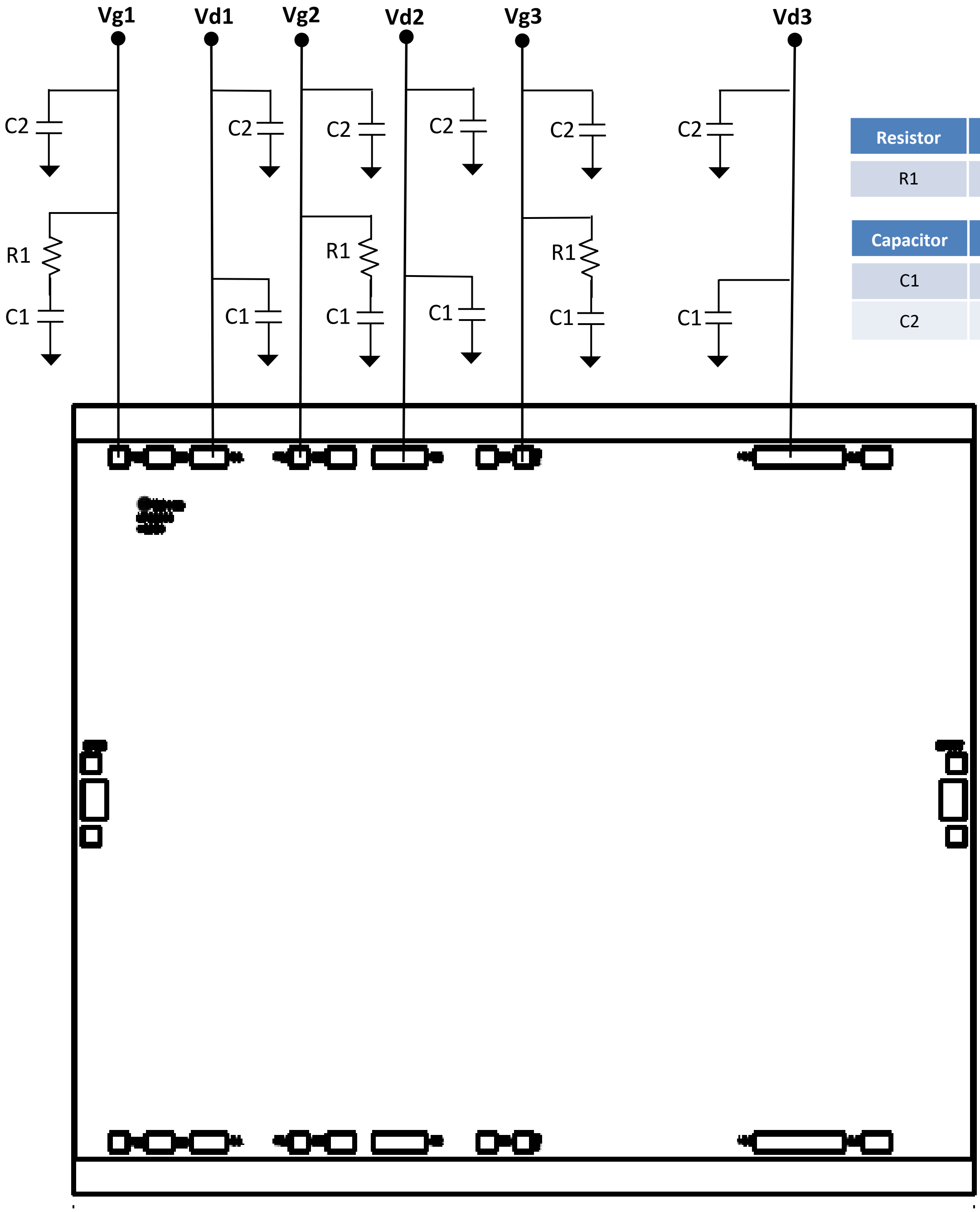
Suggested Off-Chip Components

The following diagram is a suggested bonding arraignment with off-chip components. All drain connections can be tied together to one source. All gate connections can be tied together to one source if desired. The NPA2001-TB-501 should be biased for both sides of the chip.



Resistor	Value
R1	10 Ω

Capacitor	Value
C1	0.01 µF
C2	1 µF

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Assembly Process

- The heat spreader is gold plated and can be mounted using either a high thermal conductive epoxy or solder attachment.
- Maximum recommended temperature during product attachment is 260 °C for not more than 60 seconds.
- This product contains metal air bridges so caution should be taken when handling to avoid damage.

Bias Information

Bias-up Procedure:

1.) It is recommended that voltage and current limits are set on the voltage supply's prior to biasing the product.
2.) Ensure power supplies are properly grounded to the product test fixture.
3.) Apply a negative gate voltage of -7V to Vg1, Vg2, and Vg3 to ensure all devices are pinched off.
4.) Gradually increase the drain bias voltage (Vd1, Vd2, Vd3) to the desired bias level but not to exceed the maximum voltage of 28 V.
5.) Gradually increase the gate voltages (Vg1, Vg2, Vg3) while monitoring the drain current until the desired drain current in each stage is achieved.
6.) Apply RF signal.

Bias-down Procedure:

1.) Turn off RF signal.
2.) Gradually decrease Vg1, Vg2, and Vg3 down to -7 V.
3.) Gradually decrease the drain voltages (Vd1, Vd2, Vd3) down to 0 V.
4.) Gradually increase gate voltages (Vg1, Vg2, Vg3) to 0 V.
5.) Turn off supply voltages

ESD Sensitive Product

Important Information

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